University of Rochester
Department of Electrical and Computer Engineering
Colloquia Series

Energy-efficient non-volatile memory, enabled by carbon nano-materials

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Abstract: With the advent of so-called 'abundant data' era and the required throughput and energy-efficiency for the next-generation computing paradigm, it becomes increasingly important to explore more scalable approaches for both computational (logic) and information storage (memory) devices. As illustrated in recent research articles and papers, significant progress on emerging non-volatile memory (NVM) technologies such as spin-transfer-torque magnetic random access memory (STT-MRAM), resistive RAM (RRAM), or phase-change memory (PCM), made it possible to replace the mainstream NVM (NAND Flash) and even reach certain on-chip memory requirements (e.g., L2/L3 SRAM cache). This is important, as the energy efficiency of computing circuits/systems has been increasingly limited by the memory and storage devices. In this seminar, a frontier research on the near- and long- term potential of emerging nanoscale NVM candidates will be discussed to replace today's ultimately scaled CMOS memories. The novel 1TnR (one-transistor-n-resistors) x-point memory array with carbon nanotube field-effect transistor (CNFET) as one-dimensional selection device and thus reduced sneak leakage is demonstrated as a cost-effective and 3D-stackable solution for the next-generation NVM architecture. The Al2O3-based bipolar RRAM cells are tightly integrated with the nanotube to exhibit self-compliance characteristics with high programming endurance and fast switching speed. It is pointed out that the carbon nanotube electrode brings the (lithography-free) critical dimension of the memory device down to a single-digit-nanometer. Another interesting idea of thermal engineering technique for low-power NVM cell design is also presented using a monolayer graphene (3 Å) as an interfacial thermal barrier. The RESET-programming current of the graphene-inserted PCM device is reduced by about 40%, purely due to the inserted graphene as an added thermal resistance. The status, key challenges, visions, and promising applications of the RRAM, PCM, and STT-MRAM technologies will be briefly compared and discussed in the talk.

Bio: Dr. Ahn received his Ph.D. in Electrical Engineering (EE) at Stanford University in June 2015, under the supervision of Professor H.-S. Philip Wong. He joined Stanford University in 2010, after a 3-year research career on the STT-MRAM technology with the Korea Institute of Science and Technology (KIST) in Seoul, Korea. He received the B.S. and M.S. degrees in EE from the Korea Advanced Institute of Science and Technology (KAIST) in Daejeon, Korea, in 2005 and 2007, respectively. He is the author of over 30 peer-reviewed research journal and conference papers and wrote one book chapter of Emerging Nanoelectronic Devices. His primary research interests include energy-efficient nanoscale logic and memory devices, carbon-based and other 2D-layered nano-materials, electronic/thermal/magnetic transport in nanoscale devices, and novel energy devices for beyond-CMOS domain. Dr. Ahn has been the recipient of numerous awards and honors, including John Bardeen Student Research Award for Excellence in Nanodevice Research in 2014 and Best Summer Research Intern Award by T.-C. Chen at IBM T. J. Watson in 2013.

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