University of Rochester
Department of Electrical and Computer Engineering
Colloquia Series

Spintronic & Beyond-CMOS Computing System Integration

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Computer Studies Building (CSB) 601

Abstract: Newly available materials are being evaluated as building blocks for next generation beyond-CMOS computing, and numerous devices exhibit logical functionality. The difficulty of cascading exotic nanodevices has, however, impeded large-scale computing system integration. Directly driving one device with another is particularly challenging for spintronic computing, in which electron spin is manipulated for logical switching. Further, it is important to eschew CMOS amplification and control circuits to maximally exploit emerging technologies. In this seminar, recent progress will be evaluated, with an emphasis on device interconnection, and several novel cascaded logic families will be presented. Spin-Diode Logic leverages the wide variety of magnetoresistive nanodevices controlled by magnetic fields, such as InMnAs/InAs heterojunction diodes, InSb bilayer avalanche diodes, and graphene nanoribbons. Emitter-Coupled Spin-Transistor Logic extends this concept to magnetoresistive transistors, enabling highly compact circuits. A complementary magnetic tunnel junction logic (CMAT) structure enables non-volatile computation, with charge pulses between logic gates enabling direct cascading. Additionally, multi-gate transistors are shown to provide sufficient noise margin to enable a practical threshold logic structure without requiring signal amplification circuits. These four distinct logic families and their various component nanodevices provide pathways for the replacement of CMOS for general-purpose computing. Future directions for the field of computing will also be considered, including advanced logic synthesis and proposals for bio-inspired inference circuits and spintronic FPGAs.

Bio: Dr. Joseph S. Friedman is a Research Associate with Université Paris-Sud and the French Centre National de la Recherché Scientifique. He holds a Ph.D. and M.S. in Electrical & Computer Engineering from Northwestern University and undergraduate degrees from Dartmouth College. He was a guest scientist at RWTH Aachen University, and worked on logic design automation for the Jaketown and Ivy Bridge processors as an intern at Intel Corporation. He has been awarded a Fulbright Postdoctoral Fellowship and is a member of the editorial board of the Microelectronics Journa.

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