

University of Rochester
Department of Electrical and Computer Engineering

Opportunistic Refreshing Algorithm for eDRAM Memories

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Wednesday, October 19th
12:00PM – 1:00PM
Computer Studies Building (CSB) 209

Abstract: Embedded DRAM (eDRAM) is an alternative technology that can replace SRAM cache memories. eDRAM consumes half the area and an order of magnitude less power than SRAM, but has the drawback of access blockage caused by its periodic data refreshing. This talk presents an opportunistic refreshing algorithm along with the appropriate memory architecture and skim control logic. The architecture takes advantage of the access idleness of the internal partitions of the memory and enables most of the refreshing operations to run concurrently with the ordinary R/W access. This eliminates the refreshing burden almost completely. The algorithm was simulated with industrial DSP memory access traces of CEVA Corporation, and outperformed in a wide range of eDRAM technologies and internal memory architectures.

Bio: Shmuel Wimer received his B.Sc. and M.Sc. degrees in Mathematics from Tel-Aviv University, Israel, in 1978 and 1981, respectively, and the D.Sc. degree in Electrical Engineering from the Technion-Israel Institute of Technology, in 1988. From 1978 to 2009 he worked at industry in R&D, engineering and managerial positions. From 1999 to 2009 he was with Intel, and prior to that with IBM, National Semiconductor, and IAI-Israeli Aerospace Industry. He is currently an Associate Professor with the Engineering Faculty of Bar-Ilan University, Israel. From 2011 to 2015 he was an Associate Visiting Professor in the Electrical Engineering department at the Technion. His interests include VLSI circuits and system design optimization and combinatorial optimization.

Pizza and soda will be provided