## <u>Department of Electrical and Computer Engineering</u> <u>University of Rochester, Rochester, NY</u> Ph.D. Public Defense

# Monday, February 2, 2015 4:00 PM Computer Studies Building 426

### **Power Delivery and Management in Nanoscale ICs**

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#### Abstract

The continued advance of society and emerging markets requires functionally diverse semiconductors. The future of heterogeneous, high performance systems is strongly dependent upon the power delivery system, and deeply affected by the quality of on-chip power, availability of fine grain dynamically controlled voltage levels, and the ability to manage power in real-time. To satisfy evolving power delivery requirements, an effective power delivery solution is required.

In this dissertation, a platform for scalable power delivery and management is proposed. The key concept of this platform is to manage the overall energy budget with fine grain distributed on-chip power networks, providing local feedback paths from the billions of loads to multiple, locally intelligent power routers. Essential information such as timing slacks, voltages, currents, and temperatures sensed within the individual power domains is used to locally manage power in real-time. The overall energy budget is also adjusted in a near real-time manner by communicating local power management decisions among the individual power routers within the proposed platform.

A computationally efficient methodology to co-design different types of power supplies within different levels of hierarchy has been proposed, and key circuits for distributed voltage regulation and dynamic voltage scaling have been developed. A distributed power delivery system with six ultra-small fully integrated low-dropout regulators has been fabricated in a 28 nm CMOS process and exhibits a fast transient response with excellent load regulation. To evaluate stability in a distributed power delivery system, a passivity-based stability criterion has been proposed. To provide a circuit level means for dynamically scaling the voltage in adaptive systems, a digitally controlled pulse width modulator has been developed including closed-form duty cycle expressions.

The proposed power network on-chip provides a means to efficiently deliver and intelligently manage high quality power in complex heterogeneous ICs. The issues of design complexity and scalability are addressed by providing a modular architecture that supports integration of diverse functional blocks and adapts to specific power demands without requiring re-design of the power delivery system.