Department of Electrical and Computer Engineering
University of Rochester, Rochester, NY
Ph.D. Public Defense

Friday, June 1, 2012
2:30 PM
Goergen 109

High Performance Power Delivery for Nanoscale Integrated Circuits

Selçuk Köse

Supervised by
Professor Eby G. Friedman

A critical challenge in high performance nanoscale integrated circuits is high quality power delivery. The efficient generation and distribution of multiple on-chip power supply voltages require fundamental changes to the power delivery process to provide increased current in next generation nanoscale integrated circuits. Four primary components are required to realize an efficient power delivery system: (a) ultra-small voltage converters to generate power close to the load, (b) accurate models to characterize the individual power components, (c) efficient algorithms to analyze the quality of the power delivered to the load circuits, and (d) a co-design methodology to simultaneously determine the optimal location of the on-chip power supplies and decoupling capacitors.

In this dissertation, a hybrid combination of a switching and low-dropout (LDO) regulator as a point-of-load power supply for next generation heterogeneous systems is proposed. The area of this circuit is significantly smaller than the area of conventional voltage regulators, while maintaining high current efficiency. The proposed circuit provides a means for distributing multiple local power supplies across an integrated circuit.

Another important challenge in the realization of effective power delivery systems is the analysis of this highly complicated structure where individual voltage fluctuations at millions of nodes need to be efficiently determined. Closed-form expressions for the effective resistance between circuit components have been developed. This effective resistance model is utilized in the development of a power grid analysis algorithm to compute the node voltages without requiring any iterations. This algorithm drastically improves computational complexity since the iterative procedures to determine IR drop and L di/dt noise are no longer needed.

With the introduction of ultra-small on-chip voltage regulators, there is a need for novel design methodologies to determine the location of these on-chip power supplies and decoupling capacitors. A co-design methodology is proposed to simultaneously determine the optimal location of the power supplies and decoupling capacitors within a high performance power delivery network. Optimization algorithms widely used for facility location problems are applied in the proposed methodology. The effects of the size, number, and location of the power supplies and decoupling capacitors on the power noise are also discussed.