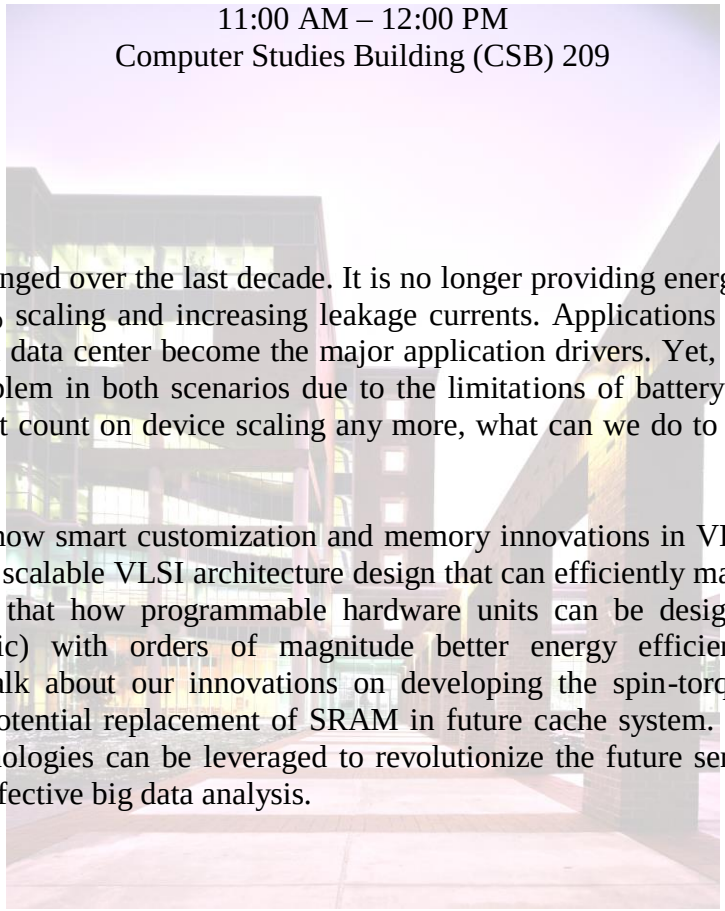
University of Rochester
Department of Electrical and Computer Engineering Colloquia

VLSI Design to The Rescue: Building Future Application Drivers with Energy Efficiency

Fengbo Ren

Wednesday, February 26th
11:00 AM – 12:00 PM
Computer Studies Building (CSB) 209



Abstract:

Technology scaling has changed over the last decade. It is no longer providing energy efficiency gains as in the past due to the end of V_{DD} scaling and increasing leakage currents. Applications have also changed. Mobile devices and server farms in data center become the major application drivers. Yet, computing energy becomes an increasingly severe problem in both scenarios due to the limitations of battery capacity and heat removal capability. While we cannot count on device scaling any more, what can we do to build the future application drivers?

In this talk, I will explain how smart customization and memory innovations in VLSI design can come to the rescue. I will first present a scalable VLSI architecture design that can efficiently maps the compressive sensing algorithms to demonstrate that how programmable hardware units can be designed to accelerate complex algorithms (domain-specific) with orders of magnitude better energy efficiency than general purpose processors. Then, I will talk about our innovations on developing the spin-torque transfer random access memory (STT-RAM)—a potential replacement of SRAM in future cache system. In the end, I will share my visions on how these technologies can be leveraged to revolutionize the future server systems for supporting energy-efficient and cost-effective big data analysis.

Bio:

Fengbo Ren received the B.S. degree in Electrical Engineering from Zhejiang University in 2008, and the M.S. degree in Electrical Engineering from the University of California, Los Angeles (UCLA) in 2010, where he is expected to receive the Ph.D. degree in summer 2014. He is interested in understanding the interplay between CMOS circuits and nano-devices, as well as the interplay between VLSI architectures and complex algorithms. Specifically, his research has been focused on designing energy-efficient VLSI systems, accelerating sparse signal processing, and developing emerging memory technology. He was with Qualcomm Inc. as an Engineer Intern in summer 2009, Cisco Systems Inc. as a Cisco Choice Ph.D. Intern in summer 2012, and Broadcom Inc. as a Fellow Intern in summer 2013, respectively. He is the recipient of 2012-2013 Broadcom Fellowship and selected as a Broadcom-UCLA fellow.

Light refreshments will be provided.