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Reliable Ultra-Low-Voltage Cache Design for Many-Core Systems

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Abstract

Energy efficiency and reliability are two main concerns in future many-core (1000+ processors) systems design. On the one hand, technology scaling makes it possible to integrate an unprecedented number of transistors on a single chip, enabling many-core system design. Unfortunately, this integration introduces energy and reliability challenges for the entire system. Additionally, as the speed gap between processor and external memory increases, large-volume, high-density caches are required, worsening reliability and energy further. An effective way to reduce power consumption is voltage scaling. However, as supply voltage decreases into the ultra-low voltage regime, the failure rate of circuits increases dramatically.

In this presentation, we exploit existing double-error correcting triple-error detecting (DECTED) codes, together with cache line disabling in an efficient way to handle both hard and soft errors. The proposed approach can reduce supply voltage beyond normally acceptable minimal supply voltage V_{DDMIN} without reducing cache reliability. We also propose a two-layer error control code, combining error detection capability of rectangular codes and error correction capability of Hamming product codes in an efficient way, in order to increase cache error resilience for many core systems, while maintaining low power, area and latency overhead. Furthermore, in order to improve system reliability amidst cache coherence, two different approaches are proposed: pre-write-back policy and uneven error-protection. Our analysis and experimental results show that our proposed methods can effectively improve energy efficiency and system reliability. For example, compared to the next-best approach in the research literature, the proposed DECTED with cache line disabling reduces system energy consumption by up to 25% and energy-execution time product by nearly 10%, while introducing only 0.28% storage overhead and marginal instruction per cycle degradation, when the target yield loss rate is 1/1000.