University of Rochester
Department of Electrical and Computer Engineering Colloquia

Beyond-CMOS Technology/Circuit Exploration for Boolean and Non-Boolean Computing Platform

Dr. Chenyun Pan

Wednesday, March 8th
12:00 PM – 1:00 PM
Computer Studies Building (CSB) 209

Abstract: Decades of continuous CMOS scaling is approaching its fundamental limits. Many beyond-CMOS device and interconnect technologies have been proposed to augment or even replace the conventional Si CMOS technology and to sustain the exponential growth of the computational power of microchips. These emerging technologies have fundamentally different operation principles, and many of them must be complemented with novel circuits, interconnect, memory, and system architecture to achieve their full potential. This requires close interaction and exploration between technology and circuit/system. Therefore, a holistic approach is in need to co-optimize different levels of abstraction. In this talk, I will start with the scaling challenges of CMOS devices and Cu/Low-k interconnects, and introduce an efficient and validated hierarchical design methodology to optimize various emerging device-, interconnect-, and system-level innovations. The importance of technology/system co-design will be addressed by several case studies. Then, I will talk about the beyond-CMOS benchmarking leadership program that I have been participating as a leading researcher. I will present a bio-inspired neuromorphic circuit, the cellular neural network (CNN), which is efficiently implemented with spintronic devices. More than 15 emerging charge- and spin-based device options will be explored and investigated based on a uniform benchmarking methodology using CNN. In the end, I will conclude the talk with future directions and research plans that will enable energy-efficient computing, such as the optimization of non-traditional majority-gate based Boolean circuits and a cross-layer optimizer for the neuromorphic computing system.

Bio: Dr. Chenyun Pan received a B.S. degree in microelectronics from the Shanghai Jiao Tong University, Shanghai, China, in 2010 and the M.S. and Ph.D. in the School of Electrical and Computer Engineering at the Georgia Institute of Technology, Atlanta, GA, in 2013 and 2015, respectively. In Summer 2014 and Spring 2015, he worked in IMEC, Belgium, as a research intern, and conducted research on ARM core optimization using multilayer graphene interconnects and deeply scaled vertical and lateral gate-all-around FETs. He is currently a research engineer in the School of Electrical and Computer Engineering, the Georgia Institute of Technology. He has over 30 peer reviewed IEEE journal and conference publications and received two best paper awards in the IEEE International Symposium on Quality Electronic Design and IEEE Conference on IC Design and Technology, respectively, as well as several best paper nominations in IEEE conferences. His research interests include the device-, circuit-, and system-level modeling and optimization for Boolean and non-Boolean computing platforms based on various emerging beyond-CMOS device and interconnect technologies.

Pizza and soda provided.