Department of Electrical and Computer Engineering
University of Rochester, Rochester, NY
Ph.D. Public Defense

Monday, July 23, 2012
10:00 AM
Computer Studies Building 426

Energy-Efficient, Wideband Transceiver Architectures and Circuits for High-Speed Communications and Interconnects

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Recently with the increasing demand for high-speed communications, wideband systems have becomes one of the major research focuses for both academia and industry. While wide bandwidth benefits high data-rate communication, compared to the conventional narrow bandwidth system, it poses large design challenges for both transceiver architectures and circuits, especially using the mainstream low cost CMOS and BiCMOS technologies. Besides, wideband systems typically inevitably require large power consumption, which might lead to worse energy-efficiency compared to the narrow-band systems. Therefore, in this thesis, we will focus on the energy-efficient, wideband transceiver architectures and circuits for high-speed communications and interconnects: ultra-wideband impulse radios (IR-UWB), intra-chip free-space optical interconnect, and on-chip electrical interconnect for multi-core processors.

Ultra-wideband communications has become an active research topic with the approval of UWB technology for commercial applications in the 3.1 - 10.6-GHz band by FCC. With such a large bandwidth, UWB technologies promise to offer low-power and high-speed wireless connectivity for future short-range communication systems. In this thesis, we will focus on the energy-efficient, wide-band UWB receiver architecture and circuits. We will first present a new UWB low-noise amplifier with noise cancelation, and use it to investigate the design trade-off for UWB amplifier. Then we will present a new analog correlation receiver architecture. It employs an energy-efficient correlator called distributed pulse correlator (DPC) for low power ultra-wideband pulse detection. Thanks to the multiple pulsed multipliers time- interleaved in a distributed fashion and built-in local template pulse generation in the DPC, the power consumption and circuit complexity are significantly reduced for the DPC-based analog correlation receiver. The operation and performance of the DPC are analyzed, and the circuit implementation of DPC is discussed in details, especially the most critical component, the pulsed multiplier. A chip prototype of the DPC-based IR-UWB receiver was implemented in a 0.18-µm standard digital CMOS technology. In the measurement, the 8-tap, 10-GSample/s DPC achieves a pulse rate of 250 MHz with an energy efficiency of 40 pJ/pulse, and the whole receiver achieves an energy efficiency of 190 pJ/pulse at the 250-MHz pulse rate. Together with a UWB transmitter and two UWB antennas, the complete IR-UWB communication link is also demonstrated.

The continuous scaling of CMOS technology enables more and more modules to be implemented into a single chip. However, it actually poses challenges in the global interconnect design, especially with the rapid demand for higher-speed communication among more modules. Conventional electrical interconnect inevitably requires significant improvement for this high-speed on-chip global communication. In this thesis, we will investigate the high-speed global interconnect through both electrical and optical options.

Optical interconnects have been recognized as a promising successor to electrical interconnects. They have advantages like large bandwidth, low latency, and less susceptible to noise. We will present a novel optical transceiver architecture and circuits for the free-space optical interconnect for high-speed intra-chip communications. Compared to the conventional embedded-clock and forwarded-clock architectures, the presented shared-clock architecture benefits low power and low design complexity on the clock generation and recovery block and a simple interface between electrics and optics. An injection-locked oscillator is employed to replace the conventional phase-locked loop as the clock generation block to further improve the energy-efficiency. Due to the high-speed and large bandwidth requirement, bandwidth extension techniques are widely used in the transceiver circuits. The optical transceiver was implemented in a 0.13-µm standard digital CMOS technology. The simulation results show that a 10-Gb/s data rate with 7.1-pJ/b energy-efficiency communication can be achieved.

For the electrical interconnect, we will present a novel on-chip interconnect system for multi-core chips using transmission lines as shared media in this thesis. It supports both point-to-point and broadcasting communications. Compared to network-on-chip approaches, it offers significant advantages in circuit complexity, energy efficiency and link latency. To demonstrate the scheme, a chip prototype with two 20-mm trans- mission lines running in parallel and multiple transmitters/receivers (including 2:1 serializer/1:2 deserializer) was implemented in a 130-nm SiGe BiCMOS technology. The transmission lines are designed with Ground-Signal-Signal-Ground configuration and patterned ground shields to exhibit low latency, small attenuation, generate less crosstalk, and provide high bandwidth density. The transceivers are designed and optimized to achieve good energy efficiency at the target data rate of 25 Gb/s. On the transmitter side, an efficient and low power pre-emphasis technique is applied to compensate for the transmission line's frequency-dependent loss. On the receiver side, latched samplers are adopted for high sensitivity. To eliminate the insertion loss caused by a dedicated isolation switch, both the transmitter and receiver are designed to be internally switched in/out from the transmission lines. The prototype can successfully demonstrate point-to-point and broadcasting communications, and can achieve a date rate of 25.4 Gb/s with an energy efficiency of 1.67 pJ/b in the measurement.