Department of Electrical and Computer Engineering
University of Rochester, Rochester, NY

Ph.D. Public Defense

Wednesday, July 1, 2015
3:00 PM
Computer Studies Building, Room 426

Energy-Efficient Architectures Based on STT-MRAM

Xiaochen Guo

Supervised by
Professor Engin Ipek

Abstract

As CMOS technology scales to smaller dimensions, leakage concerns are starting to limit microprocessor performance growth. To keep dynamic power constant across process generations, traditional MOSFET scaling theory prescribes reducing supply and threshold voltages in proportion to device dimensions, a practice that induces an exponential increase in subthreshold leakage. As a result, leakage power has become comparable to dynamic power in current-generation processes, and will soon exceed it in magnitude if voltages are scaled down any further.

The rise in sub-threshold leakage also has an adverse effect on the scaling of semiconductor memories. DRAM density scaling has become increasingly difficult due to the challenges in maintaining a sufficiently high storage capacitance and a sufficiently low leakage current at nanoscale feature sizes. Non-volatile memories (NVMs) have drawn significant attention as potential DRAM replacements because they represent information using resistance rather than electrical charge. Spin-torque transfer magnetoresistive RAM (STT-MRAM) is one of the most promising NVM technologies due to its low write energy, high speed, and high endurance.

This dissertation presents a new class of energy-efficient processor and memory architectures based on STT-MRAM. By implementing much of the on-chip storage and combinational logic using leakage-resistant, scalable RAM blocks and lookup tables, and by carefully re-architecting the pipeline, an STT-MRAM based implementation of an eight-core Sun Niagara-like processor reduces chip-wide power dissipation by 1.7x and leakage power by 2.1x at the 32nm technology node, while maintaining 93% of the system throughput of a CMOS-based design.

A new memory architecture, *Sanitizer*, is introduced to make STT-MRAM a viable DRAM replacement for main memory. Sanitizer addresses *retention errors*, one of the most critical scaling problems of STT-MRAM. As the size of the storage element within an STT-MRAM cell decreases with technology scaling, STT-MRAM retention errors are expected to become more frequent, which will require multi-bit error-correcting code (ECC) and periodic scrubbing mechanisms. Sanitizer mitigates the performance and energy overheads of ECC and scrubbing in future STT-MRAM based main memories by anticipating the memory regions that will be accessed in the near future and scrubbing them in advance. It improves performance by 1.22x and reduces end-to-end system energy by 22% over a baseline STT-MRAM system at 22mm.