Data Bus Swizzling in TSV-Based Three-Dimensional Integrated Circuits

by

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Curriculum Vitae

The author was born in Hebei, China on June 3rd, 1989. She attended South China University of Technology from 2006 to 2010, and graduated with a Bachelor of Engineering degree in 2010. She arrived at the University of Rochester in the fall of 2010 and began graduate studies in VLSI/IC design. She pursued her research in designing 3-D TSV-based data bus structures under the direction of Prof. Eby G. Friedman.

Acknowledgment

I feel very grateful that I could have the opportunity to work with my advisor, Professor Eby G. Friedman. It is he who teaches me the right way to do research. His expertise in VLSI field and wisdom on life deserve everyone's trust. His responsibility and patience to students worth everyone's respect. Everything I have learnt from Professor Friedman will be the treasure for my whole life.

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I would also like to thank Zhuang Hou from the Department of Mathematics for his sensible suggestions regarding the work described in Chapter 2.3.

Abstract

The purpose of this thesis is to efficiently exploit swizzling in reducing coupling noise between the bit lines of a TSV data bus in three-dimensional integrated circuits (3-D ICs). The core concept of swizzling is to distribute the noise of an aggressor to all victims, instead of merely concentrating on the nearest victim. Based on this principle, an optimal swizzling pattern, which is signal dependent, is proposed. The physical circuit model is simulated in HSPICE. The reduction in peak coupling noise is evaluated for different parameters, including the TSV diameter (D), aspect ratio (AR), and transition time (TR) of the aggressor signal. A maximum reduction in peak coupling noise of 51.4% is achieved. An explanation of the HSPICE simulation results is provided. A MATLAB model, based on the physical parameters of a TSV, is also described to exploit the effect of TSV pitch on the performance of swizzling. The validity of this MATLAB model is also verified through HSPICE simulations. Overall, the application of swizzling to 3-D TSV data buses is discussed, and the swizzling pattern that minimizes peak coupling noise is provided.

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Foreword

Chapter 1, Expressions (1.1) - (1.14): the closed-form expressions of 3D via resistance, inductance, and capacitance used throughout the thesis were developed by Professor Eby G. Friedman and Ioannis Savidis.

Chapter 1, Decoupling technique: the technique referred throughout the thesis was developed by Professor Eby G. Friedman and Junmou Zhang.

Introduction

With the increasing need for high performance electronic devices, the semiconductor industry is integrating more modules onto an integrated circuit (IC) [1]. The area of one die therefore keeps growing, increasing the length of the long interconnects. One severe consequence of this issue is the effect on the data bus. Non-negligible parasitic impedances between long data buses produce intolerable delay and noise, which severely harms the performance of a data bus. Methods to reduce these effects have been proposed [2]-[8]. There is a need, however, for circuit techniques that will enhance circuit performance such as power efficiency and high speed with small area.

Three-dimensional integrated circuits (3-D ICs) are a promising circuit technique. A 3-D structure can exhibit advantages such as high speed, parallel signal processing, and high packaging density [1]. To achieve these advantages, a highly efficient data bus is necessary to guarantee the speed and accuracy of the intra-layer communication. In a 3-D IC, the vertical signals propagate across the through silicon vias (TSVs). The short length and regular shape of a TSV support the function of a data bus. However, as scaling technology shortens the distance between adjacent bit lines in a data bus [9], [10], capacitive and inductive coupling become more significant. To maximize the priority of a TSV as a data bus, swizzling [11], [12] is applied.

Swizzling is a method to route interconnects to reduce crosstalk noise [13]-[16]. This technique has been used in 2-D ICs but not yet in 3-D ICs. To satisfy the needs of the market, the number of layers in a 3-D IC will continue to increase. This issue will affect data buses in 3-D ICs in a similar manner as in 2-D ICs. Therefore, applying swizzling to a 3-D TSV-based data bus is effective in lowering the peak noise between adjacent wires. Swizzling, however, does not function well under all conditions. Factors such as the TSV impedance, TSV pitch, and signal propagated along the line affect the efficiency of swizzling. Hence, it is necessary to produce a method to distinguish the boundaries where the performance of a swizzled data bus exceeds a non-swizzled data bus.

The primary goal of swizzling within a data bus is to reduce the peak coupling noise induced by an aggressor line. As compared to the non-swizzling case, a swizzled data bus has a more complicated structure which exhibits larger parasitic impedances. This tradeoff needs to be balanced to minimize the peak coupling noise. A method to determine the most efficient swizzling pattern is developed. The validity of this method is demonstrated through HSPICE simulations.

This thesis is composed of three chapters. Background knowledge about data buses, 3-D ICs, TSVs, and swizzling is introduced in Chapter 1, laying the foundation for the following chapter. In Chapter 2, the efficiency of the proposed swizzling pattern is demonstrated through HSPICE and MATLAB simulations. The research is summarized and some future research ideas are suggested in Chapter 3.

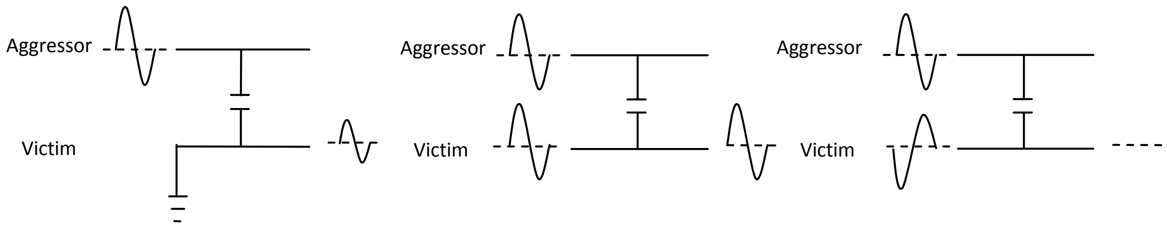
Chapter 1

In this chapter, background knowledge about 3-D ICs, TSVs, TSV-based data buses, and swizzling is introduced. A signal independent swizzling pattern, minimizing the peak coupling noise, is proposed.

1.1 Data bus

A data bus carries data to facilitate the communication within the CPU, memory, and peripherals. To achieve high speed and accurate communication, the data bus needs to exhibit low delay and high signal integrity. A shorter time of flight, however, does not mean that the physical length of a data bus is shorter.

A data bus can be categorized in terms of either a parallel data bus or a serial data bus. A parallel data bus simultaneously carries data words on multiple wires. The width of a modern parallel data bus typically varies from 8 bits to 128 bits or more. These parallel lines can interact, resulting in crosstalk coupling noise [17].



(a) (b) (c)

Figure 1.1: Crosstalk when a) victim is grounded, b) victim phase is the same as the aggressor, and c) victim phase is opposite to the aggressor.

Crosstalk is described as a signal affecting an adjacent nearby signal through capacitive or inductive coupling [18], [19]. The parasitic impedance causes a larger delay on both the aggressor and victim lines [20], [21]. Signal integrity on the victim line can also be affected, as shown in Figure 1.1.

In addition to crosstalk, a parallel data bus can also exhibit clock skew issues. As shown in Figure 1.2, in a synchronous circuit, the clock does not simultaneously arrive at two sequentially-adjacent registers. This time difference is called clock skew [22]. Sequentially-adjacent registers mean that there is only combinational logic or interconnects between the two registers [22]. The cause of clock skew is the different delay from the clock source to the individual registers. Each bit of a parallel data bus ideally switches at the same time as a single clock event. The wider the data bus, the more likely the clock reaches the driver of each bit line at a different time, which suggests a higher risk of clock skew. Hence, an asymmetric clock network with an asymmetric impedance distribution can directly cause clock skew. In some cases, clock skew can lead to a violation in the hold and setup times, affecting circuit behavior [23], [24].

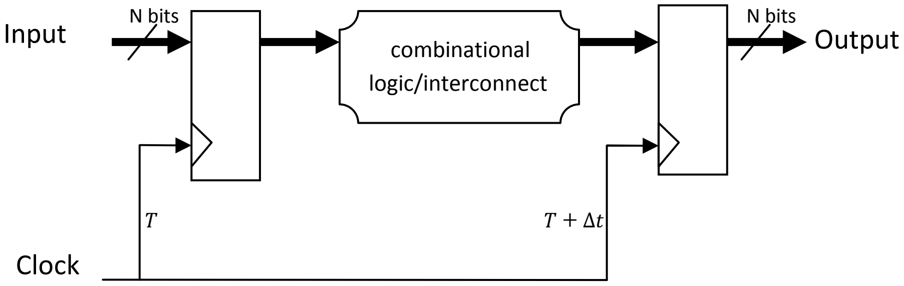


Figure 1.2. Clock skew in a sequential circuit.

Both crosstalk and clock skew can have a negative effect on signal integrity in a parallel data bus. A serial data bus which only contains one bit line does not exhibit timing skew or crosstalk issues, but requires a higher frequency to satisfy the bandwidth requirement [25]-[27]. Due to the high speed and low power consumption requirements of most data buses, a parallel structure is therefore widely applied in industry.

1.2 Three-dimensional integrated circuits (3-D ICs)

A 3-D IC is a stacked structure of wafers or dies [28]. Each layer of a 3-D IC can offer a particular function. For example, the top layer can be a memory while an adjacent layer can be a microprocessor. While the number of layers keeps increasing, one 3-D IC can achieve more complex functions at a faster speed [29].

As compared to a two-dimensional integrated circuit (2-D IC), a three-dimensional integrated circuit (3-D IC) has shorter wire lengths [30]. Assume there are N square modules within a 2-D IC and 3-D IC, the area of each square module is 1 unit. As shown in Figure 1.3, for the 2-D IC, the entire area is N units. For the 3-D IC, if there are N layers, the area of this 3-D IC is 1 unit. The side of each layer of the 3-D IC is 1 unit while the 2-D IC is $\sqrt{N}$ units. The wire length on each die of an N layer 3-D IC is therefore reduced to $\frac{1}{\sqrt{N}}$. According to the empirical formula of wire delay $t_d = 0.35rcl^2$ [31], the propagation time of a 3-D IC is reduced by $\frac{1}{N}$.

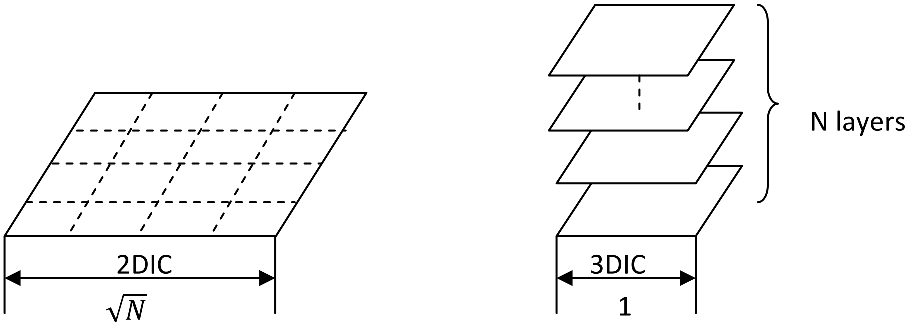


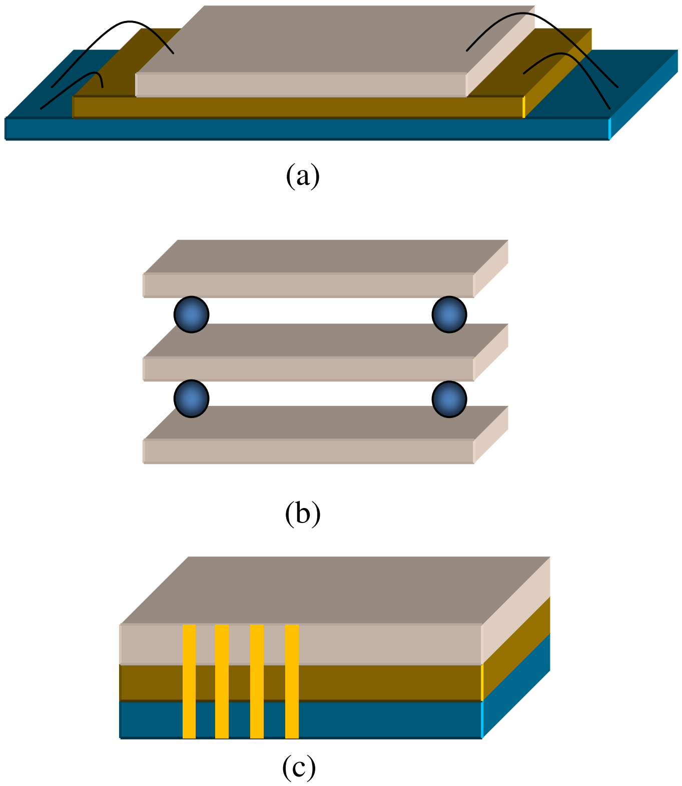
Figure 1.3. Comparison of 2-D IC with 3-D IC area.

Each die within a 3-D stack can be tested before assembling. The pre-checked die is named Known Good Die (KGD). This pre-checking process of 3-D ICs is called a KGD strategy [32]. The KGD strategy can only be used for die-level stacking while most of the modern 3-D IC manufacturing technique is at the wafer level [33]. However, with the development of related techniques, a die level 3-D IC manufacturing technique can improve yield with the KGD strategy [34].

3-D ICs are amenable to parallel processing [34]. As each layer of a 3-D IC can be considered as an individual module, it is feasible to separately manufacture each module. This parallel manufacturing process increases the speed of the entire 3-D production process.

To enhance the design of 3-D ICs, highly efficient connections among device layers are necessary. Wired connections, such as wire bonding, bumps, and through silicon vias (TSVs) have been used in integrated circuits for a long time [35], [36]. Wire bonding, as shown in Figure 1.4(a), is a mature technique which is less appropriate for scaling ICs due to length and spacing requirements. A bump, as shown in Figure

1.4(b), is another method to connect layers. However, the existence of bumps results in a discontinuous data path, which causes impedance mismatch and signal reflections [37]. Through silicon vias (TSVs), as shown in Figure 1.4(c), require shorter lengths, less space, and a continuous data path, making TSVs a promising technique for 3-D ICs.


(a)

(b)

(c)

Figure 1.4: Wired connections, a) wire bonding, b) bumps, and c) TSV.

1.3 Through silicon via (TSV)

In this section, the impedance characteristics of a through silicon via are introduced. In addition, the application of TSVs to a data bus, and related issues such as skin and proximity effects, structures of TSV data buses, and decoupling techniques are discussed. A description of the swizzling concept applied to a data bus is also provided. A method to determine the optimal swizzling pattern to minimize the peak coupling noise is also proposed.

1.3.1 Categories of TSVs

The key difference between 3-D integration and 3-D packaging is that vertical communication of the former technique is based on TSVs [38], [39]. The formation process of a through silicon via (TSV) contains patterning, etching (wet or laser), isolation/seed/barrier (conformal and continuous deposition), and filling (copper, gold, polysilicon, or glass [40]). The state-of-art in 3-D manufacturing achieves a small pitch (typically ranging between 130 and 200 μm), which supports a high density, parallel TSV data bus [40].

There are two kinds of TSVs with respect to the thickness of the substrate: thick and thin. A thick rigid substrate (a typical height is up to 600 μm [40]) avoids the need for an organic substrate. A thick TSV has two main drawbacks: first, the via resistance and capacitance are larger, resulting in a larger parasitic impedance; secondly, the thick substrate increases the height of the package (the height can be greater than 200 μm). Conversely, a thin substrate (a typical height ranges between 100 and 200 μm [40]) avoids severe capacitive or inductive coupling due to the low via impedance.

An advantage of a TSV is the potential utility for thermal control [28], [41]. A TSV can function as a heat sink or channel to disperse heat. As a TSV data bus vertically crosses all layers, the heat produced within a dense data bus can be distributed to the other layers. These characteristics reduce the deleterious effects of high temperatures such as high thermal densities [42].

1.3.2 TSV impedances

There are mainly five types of impedances characterizing a TSV data bus: self-resistance R_{self}, self-capacitance C_{self}, self-inductance L_{self}, coupling capacitance $C_{coupling}$, and mutual inductance L_{mutual}. Closed-form expressions characterizing these parameters have been developed [43]. The value of these parameters applied within an HSPICE circuit model is determined from the following formulae,

$$R_{self} = \frac{1}{\sigma_w}\frac{L}{\pi R^2}, \tag{1.1}$$

where R is the radius of a TSV and L is the length of a TSV. σ_w is the conductivity of the filled materials. The conductivity of tungsten is assumed here to be 1.79×10^7 S/m.

$$\alpha = \begin{cases} 1 - e^{\frac{-4.3L}{D}}, & if\ f = DC \\ 0.94 + 0.52e^{-10\left|\frac{L}{D}-1\right|}, & if\ f > f_{asym}, \end{cases} \tag{1.2}$$

where f_{asym} is within the intermediate frequency zone, 200 to 800 MHz [43], when the self-inductance of a TSV begins to decrease.

$$\beta = \begin{cases} 1, & if\ f = DC \\ 0.1535 \ln \frac{L}{D} + 0.592, & if\ f > f_{asym}\,, \end{cases} \tag{1.3}$$

$$DC\colon \begin{cases} L_{self} = \alpha \frac{\mu_0}{2\pi}\left[\ln\left(\frac{L+\sqrt{L^2+R^2}}{R}\right)L + R - \sqrt{L^2+R^2} + \frac{L}{4}\right] \\ L_{mutual=}\beta\frac{\mu_0}{2\pi}\left[\ln\left(\frac{L+\sqrt{L^2+P^2}}{P}\right)L + P - \sqrt{L^2+P^2}\right], \end{cases} \tag{1.4}$$

$$f_{asym}\colon \begin{cases} L_{self} = \alpha\frac{\mu_0}{2\pi}\left|\ln\frac{2L}{R} - 1\right| L \\ L_{mutual=}\beta\frac{\mu_0}{2\pi}\left[\ln\left(\frac{L+\sqrt{L^2+P^2}}{P}\right)L + P - \sqrt{L^2+P^2}\right], \end{cases} \tag{1.5}$$

α and β, used in (1.4) and (1.5), are provided, respectively, in (1.2) and (1.3). t_0 is the thickness of the barrier and S is the separation of two adjacent TSVs. The TSV pitch P is expressed as $P = S + 2(R + t_0)$. μ_0 is the permeability of air with a value of $4\pi \times 10^{-7}$ H/m.

$$C_{self} = \alpha\beta \cdot \frac{\epsilon_{SiO_2}}{t_{diel} + \frac{\epsilon_{SiO_2}}{\epsilon_{Si}} x_d T_p} 2\pi R L, \tag{1.6}$$

$$x_{dT_p} = \sqrt{\frac{4\epsilon_{Si}\emptyset_{f_p}}{qN_A}}, \tag{1.7}$$

$$\emptyset_{f_p} = V_{th}\ln\left(\frac{N_A}{n_i}\right), \tag{1.8}$$

$$\alpha = \left(-0.0351\frac{L}{D} + 1.5701\right) S_{gnd_{\mu m}}^{0.0111\frac{L}{D} - 0.1997}, \tag{1.9}$$

$$\beta = 5.8934 D_{\mu m}^{-0.553} \left(\frac{L}{D}\right)^{-(0.0031 D_{\mu m} + 0.43)}. \tag{1.10}$$

α and β, used in (1.6), are provided in (1.9) and (1.10). x_{dT_p} is the depletion region depth, $\emptyset_{f_p}$ is the p-type silicon work function, and N_A is the doped acceptor concentration with a value of 10^{21} m^{-3}. n_i is the intrinsic semiconductor concentration with a value of 1.5×10^{16} m^{-3}. The thermal voltage V_{th} is $\frac{kT}{q}$. When $T = 300$ K, the value is 25.9 mV. The silicon permittivity is $11.7 \times 8.85 \times 10^{-12}$ F/m, and the permittivity of SiO_2 is $3.9 \times 8.85 \times 10^{-12}$ F/m. t_{diel} is the thickness of the dielectric, which is assumed to be 100 nm. S_{gnd} is the distance of a TSV to the ground plane, where 10 μm is assumed.

$$C_{coupling} = 0.4\alpha\beta\gamma \cdot \frac{\epsilon_{Si}}{S}\pi DL, \tag{1.11}$$

$$\alpha = 0.225 \ln\left(0.97\frac{L}{D}\right) + 0.53, \tag{1.12}$$

$$\beta = 0.5711\left(\frac{L}{D}\right)^{-0.988} \ln\left(S_{gnd_{\mu m}}\right) + \left(0.85 - e^{-\frac{L}{D}+1.3}\right), \tag{1.13}$$

$$\gamma = 1. \tag{1.14}$$

$\alpha, \beta,$ and γ, used in (1.11), are provided, respectively, in (1.12), (1.13), and (1.14).

1.4 TSV data bus

In this section, commonly encountered problems in wide interconnects, such as the proximity and skin effects, are introduced. The structure of a TSV data bus, including parallel column and bundle, is described. A discussion of clock skew and coupling noise in a TSV data bus is also presented. Finally, a decoupling technique is applied to determine the parasitic impedances.

1.4.1 Skin and proximity effects

The skin effect, shown in Figure 1.5, occurs when a conductor carries an alternating current. The current flow tends to concentrate near the surface. When the frequency of the propagated signal is high and the section of the conductor is large, the skin effect can be significant [44]. As the unevenly distributed current can increase the effective resistance of the conductor, the propagation delay is also increased and the power consumption becomes larger [45]-[47].

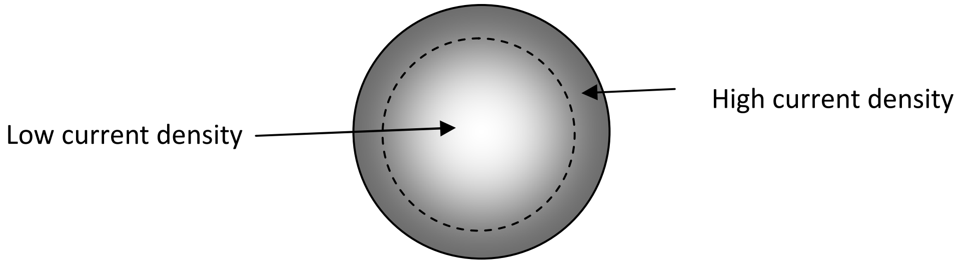


Figure 1.5. Skin effect.

The proximity effect, shown in Figure 1.6, occurs when a conductor carries an alternating current and produces an alternating magnetic field. The current distribution within an adjacent conductor concentrates within a small region. When the currents pass in opposite directions, the current in an adjacent conductor concentrates at the nearest side to the aggressor conductor; when the currents pass in the same direction, the current concentrates at the farther side [44].

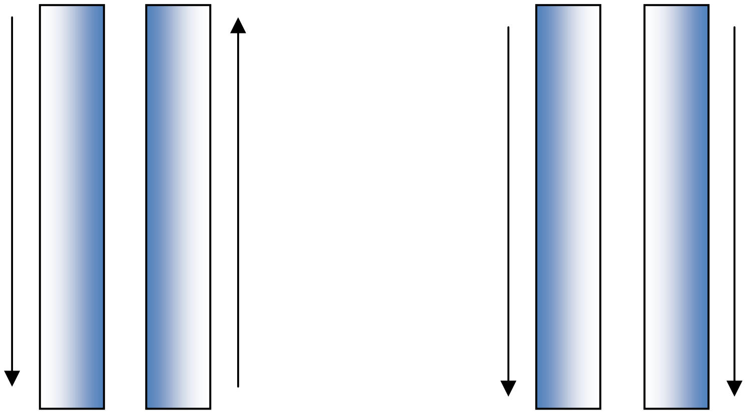


Figure 1.6. Proximity effect.

Because of skin and proximity effects, the inductance and capacitance of the conductor are frequency dependent [48]. The unevenly distributed current can shorten the lifetime of a conductor [49], [50]. The total length of a vertical TSV data bus is the summation of the thickness of each of the layers. As compared to a horizontal data bus in a 2-D IC, a 3-D TSV data bus can achieve a shorter signal propagation time. In addition, a TSV is a cylinder shaped conductor, where the diameter and pitch can be manufactured to avoid significant proximity and skin effects [51].

1.4.2 Structure of a TSV data bus

As shown in Figure 1.7, a TSV data bus is formed from two kinds of structures: parallel column and bundle [52]. The TSV pitch in these two structures is assumed to be 1 unit. For a nine bit parallel column structure, the longest distance between two registers is eight units while for a nine bit bundled pattern, the longest distance between two registers is $2\sqrt{2}$ units.

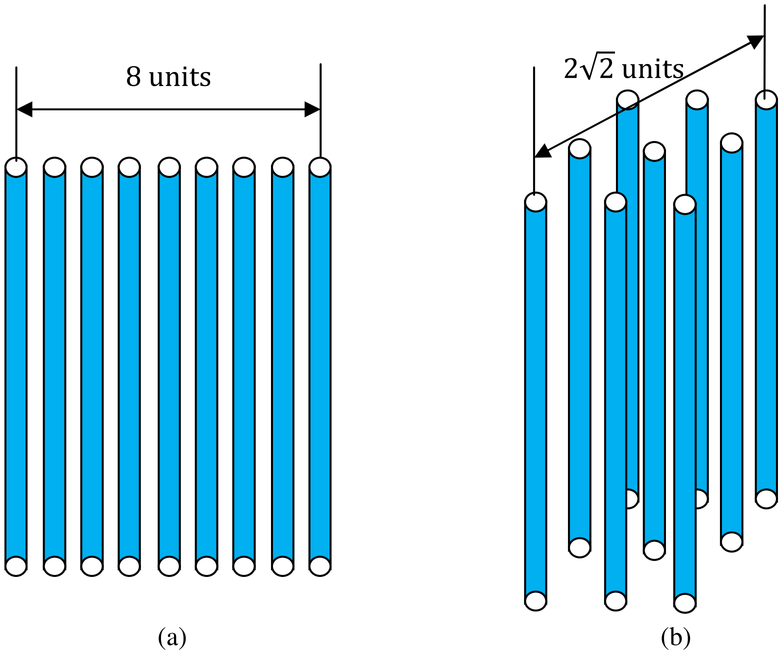


Figure 1.7: Structure of TSV data buses, a) parallel column, and b) bundle.

In a data bus, each bit line is synchronized by the same clock. Due to the asymmetry of a clock network, it is difficult to guarantee that the clock signal reaches the driver of each bit line at the same time. The skewed time can result in asynchronization of the signals. For the worst case, the output word can be misrepresented. The risks of timing skew increase with the width of the data bus. Although timing skew cannot be completely removed, a bundled structure produces lower timing skew as compared to a parallel column structure.

The timing skew issue in a four bit TSV data bus with a parallel column structure is illustrated in Figure 1.8. Due to the asymmetry of the clock tree, the clock signal arrives at pass gate P0 and P3 at different times. If this timing skew is sufficiently large, the input signals in0 and in3 will pass through the respective pass gate to the data bus within different clock cycles, which can lead to misrepresentation of a word.

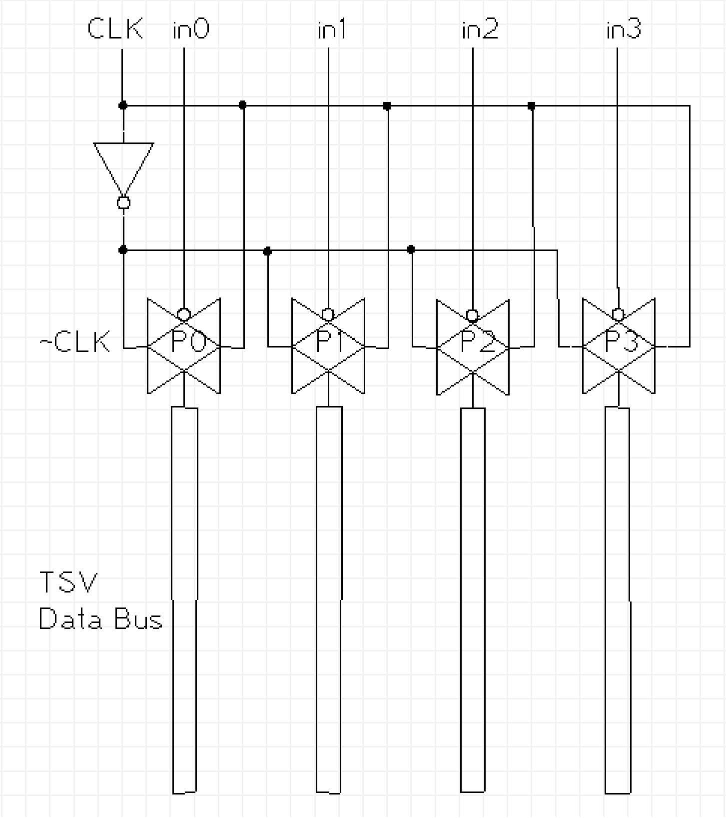
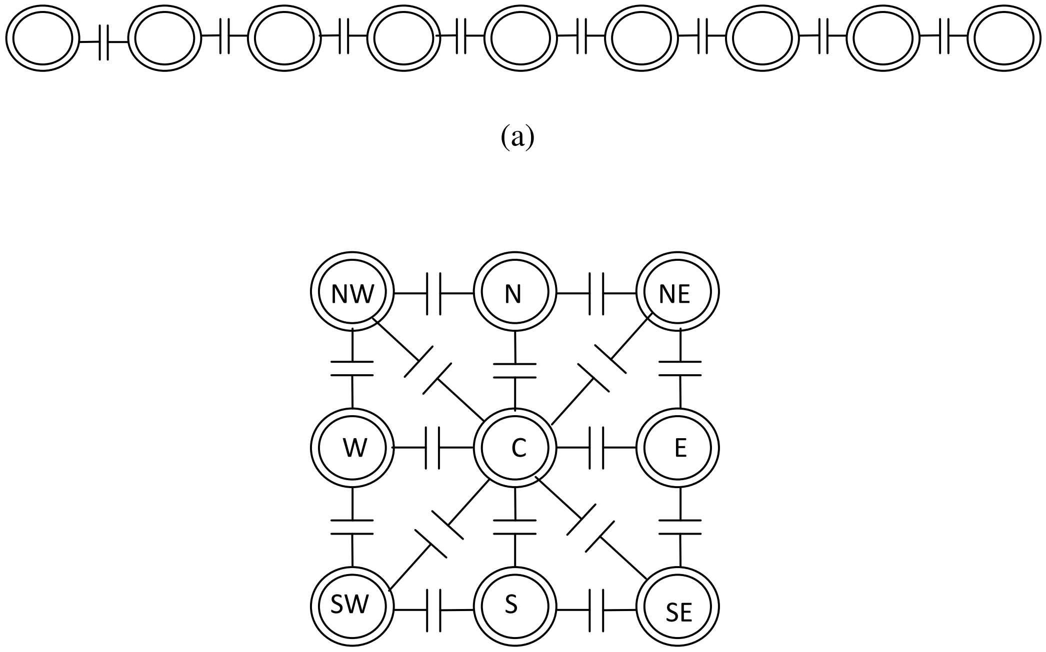


Figure 1.8. Timing skew in a four bit parallel column TSV data bus.

The top view of a nine bit parallel column TSV data bus and a nine bit bundle TSV data bus are shown in Figure 1.9. In the parallel column pattern, each TSV has at most two adjacent TSVs; in a bundled pattern, the center TSV has eight adjacent TSVs. The effects of both capacitive and inductive coupling in a bundled TSV data bus are more significant than in a parallel column structure [53].



(a)

(b)

Figure 1.9: Coupling effects in a TSV data bus, top view of a) parallel column data bus, and b) bundled data bus.

Severe timing skew can be avoided in a bundled structure while a parallel column structure exhibits less coupling. Swizzling in a bundled structure [54] has been considered, but does not provide a specific method to maximize the efficiency of swizzling. Due to the high complexity of the coupling situation in a TSV bundle, the research described in this thesis focuses on the parallel column TSV data bus.

1.4.3 Decoupling of TSVs

An analysis of the impedance of each bit line within a TSV data bus is necessary to explain the HSPICE simulation results. The mutual inductance and coupling capacitance within the bit lines of a parallel data bus, however, increase the complexity of the analysis. Several decoupling methods have been proposed [55]-[57]. The method provided in [57] is applied to decouple between adjacent TSV bit lines of a data bus. The procedure is to initially obtain the Kirchhoff equation describing two coupled TSVs and determine the transfer matrix E of the input and output. The transfer matrix *E* is then diagonalized to *E'*. Based on the new transfer matrix *E',* the output of the two coupled TSVs can be determined from the transfer function of two independent TSVs, $H_1(s)$ and $H_2(s)$. Finally, based on $H_1(s)$ and $H_2(s)$, the structure of the decoupled TSVs is obtained. The decoupling process among the bit lines of a TSV data bus is illustrated in Figure 1.10.

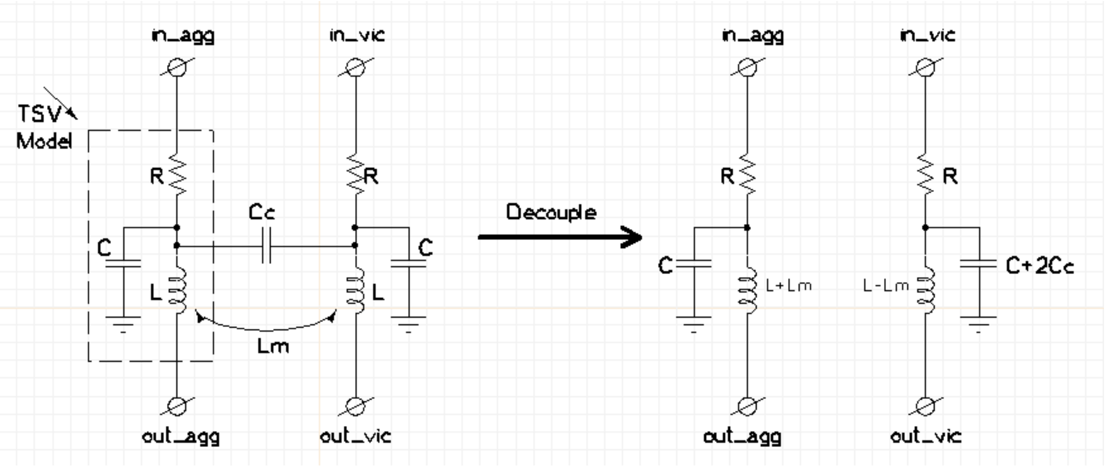


Figure 1.10. Decoupled TSV pair.

After decoupling, the mutual inductance and capacitance are distributed to two independent TSV bit lines. The self-inductance and self-capacitance of the decoupled aggressor line are, respectively, $L + L_m$ and C, while the decoupled victim line is, respectively, $L - L_m$ and $C + 2C_c$.

1.5 Swizzling

In this section, an explanation of the swizzling concept is provided. The process to apply swizzling into a TSV data bus is also illustrated. Some discussion about the limitations and potential of the TSV data bus with swizzling method is discussed.

1.5.1 The concept of swizzling

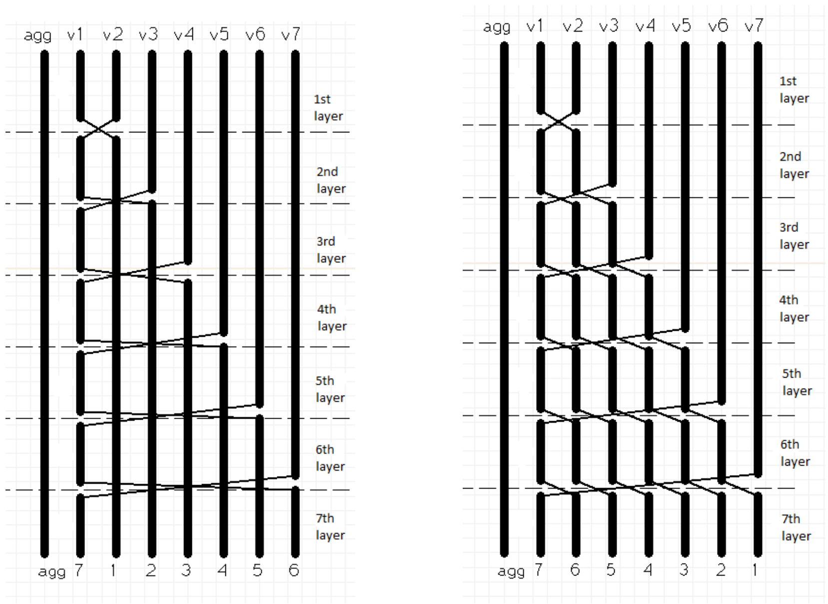
Swizzling is a method of changing the data paths to reduce crosstalk noise. It is necessary to first distinguish two concepts: local coupling and global coupling. These two coupling cases are dependent on the length and distance of the coupled signal paths. Local coupling describes the coupling of a segment of the whole signal path. Alternatively, global coupling describes the coupling of the entire signal path. The coupling situation is determined by the mutual capacitance and inductance, which is characterized as a parasitic impedance. Hence, the parasitic impedance of a segment of the signal path can represent local coupling, while the parasitic impedance of the entire path can describe global coupling.

The core concept of swizzling is to distribute the influence of an aggressor onto all of the victims instead of concentrating on the nearest victim. An aggressor line induces the largest coupling noise on the nearest victim. Each time a victim line is adjacent to an aggressor, the local parasitic coupling impedance is greatest, making the local coupling temporarily more significant. As the mutual inductance and capacitance decrease when the distance increases, the coupling becomes weaker as the victim line is placed farther from the aggressor line. The local coupling noise on the victim is then less. Although the local coupling capacitance can temporarily increase the local noise, the noise at the output is reduced after applying swizzling.

Swizzling changes the impedance of each data path. One intuitive assumption of the most efficient swizzling pattern is that the pattern needs to exhibit an evenly distributed impedance of each bit line after decoupling, which means the impedance of each individual bit line is similar. The reason to guarantee this “even” property is that the speed of a data bus is subject to the slowest bit line. An uneven impedance distribution can result in a high impedance line which can slow the entire data bus. Alternatively, a parallel data bus with evenly distributed impedances makes the bus speed unconstrained by any particular slow bit line.

1.5.2 Determination of optimal swizzling

The idea of swizzling is to distribute the noise of the aggressor to all victims, instead of merely concentrating on the nearest victim. Based on this principle, two intuitive swizzling patterns are proposed, as shown in Figure 1.11. An eight bit TSV data bus is assumed to cross a seven layer 3-D IC. All the patterns are swizzled six times, which makes each victim line adjacent to the aggressor line only once. The difference among these two patterns is: in pattern I, during each swizzling, only two victim signal paths change directions while the other paths maintain the original directions; in pattern II, the more times swizzling is applied, the more victim signal paths change directions. Swizzling occurs each time when the signals are propagated from one layer to the next adjacent layer.



(a) (b)

Figure 1.11: Swizzling patterns, a) pattern I, and b) pattern II.

The signal paths can be described with a 7 × 8 matrix. The signal path of swizzling pattern I is

$$\begin{bmatrix} agg & v1 & v2 & v3 & v4 & v5 & v6 & v7 \\ agg & v2 & v1 & v3 & v4 & v5 & v6 & v7 \\ agg & v3 & v1 & v2 & v4 & v5 & v6 & v7 \\ agg & v4 & v1 & v2 & v3 & v5 & v6 & v7 \\ agg & v5 & v1 & v2 & v3 & v4 & v6 & v7 \\ agg & v6 & v1 & v2 & v3 & v4 & v5 & v7 \\ agg & v7 & v1 & v2 & v3 & v4 & v5 & v6 \end{bmatrix}, \tag{1.15}$$

and signal path of swizzling pattern II is

$$\begin{bmatrix} agg & v1 & v2 & v3 & v4 & v5 & v6 & v7 \\ agg & v2 & v1 & v3 & v4 & v5 & v6 & v7 \\ agg & v3 & v2 & v1 & v4 & v5 & v6 & v7 \\ agg & v4 & v3 & v2 & v1 & v5 & v6 & v7 \\ agg & v5 & v4 & v3 & v2 & v1 & v6 & v7 \\ agg & v6 & v5 & v4 & v3 & v2 & v1 & v7 \\ agg & v7 & v6 & v5 & v4 & v3 & v2 & v1 \end{bmatrix}. \tag{1.16}$$

Each layer of a TSV data bus is considered as a group of parallel columns, where the inductance and capacitance of each bit line after decoupling is provided, respectively, in (A.1.9) – (A.1.16) and (A.1.17) – (A.1.18). As listed in Table A.1, for pattern I, the signal path with the maximum inductance is $v1$ with a value of $(7L_{self} + L_{m2} + 7L_{m3} + 7L_{m4} + 7L_{m5} + L_{m6})$, where L_{self} is the self-inductance and L_{mi} is the mutual inductance between two TSVs when the spacing equals i times the pitch. The signal path having the minimum inductance is $v7$ with a value of $(7L_{self} - 6L_{m1} - 5L_{m2} - 5L_{m3} - 5L_{m4} - 5L_{m5} - 5L_{m6} - 6L_{m7})$. For pattern II, the signal path having the maximum inductance is $v3$ with a value of $(7L_{self} + L_{m2} + L_{m3} + 3L_{m4} + L_{m5} + L_{m6})$, which is less than pattern I. The signal path having the minimum inductance is also $v7$ with a same value as pattern I. As compared to pattern I, the difference between the maximum and minimum inductance of signal path in pattern II is smaller, suggesting a more symmetric impedance distribution. This comparison provides a hint for determining the optimal swizzling pattern, which should exhibit the most symmetric impedance distribution. In the optimal pattern, the inductance of each victim signal path is the same. The process of achieving this symmetric distribution is listed in Table 1.1. As the first bit line is the aggressor signal, it is not shown.

Table 1.1. Symmetric inductance distribution

	$v1$	$v2$	$v3$	$v4$	$v5$	$v6$	$v7$
Layer 1	L1	L2	L3	L4	L5	L6	L7
Layer 2	L7	L1	L2	L3	L4	L5	L6
Layer 3	L6	L7	L1	L2	L3	L4	L5
Layer 4	L5	L6	L7	L1	L2	L3	L4
Layer 5	L4	L5	L6	L7	L1	L2	L3
Layer 6	L3	L4	L5	L6	L7	L1	L2
Layer 7	L2	L3	L4	L5	L6	L7	L1

As shown in Table 1.1, each row contains L1 to L7, showing that the seven victim signals pass through seven bit lines in each layer. Each column also contains L1 to L7, but with a different sequence. The summation of inductance for each signal path is made to be the same with a value of $(7L_{self} - L_{m7} - L_{m6} - L_{m5} - L_{m4} - L_{m3} - L_{m2} - L_{m1})$, as listed in Table A.1. As compared to swizzling patterns I and II, this optimal pattern exhibits an evenly distributed impedance with a smaller maximum inductance. The signal path can also be described by a 7 × 8 matrix,

$$\begin{bmatrix} agg & v1 & v2 & v3 & v4 & v5 & v6 & v7 \\ agg & v7 & v1 & v2 & v3 & v4 & v5 & v6 \\ agg & v6 & v7 & v1 & v2 & v3 & v4 & v5 \\ agg & v5 & v6 & v7 & v1 & v2 & v3 & v4 \\ agg & v4 & v5 & v6 & v7 & v1 & v2 & v3 \\ agg & v3 & v4 & v5 & v6 & v7 & v1 & v2 \\ agg & v2 & v3 & v4 & v5 & v6 & v7 & v1 \end{bmatrix}. \tag{1.17}$$

Based on (1.17), the structure of a data bus with an optimal swizzling pattern is illustrated in Figure 1.12. The concept of this optimal pattern is applied to an N bit TSV data bus in the following section.

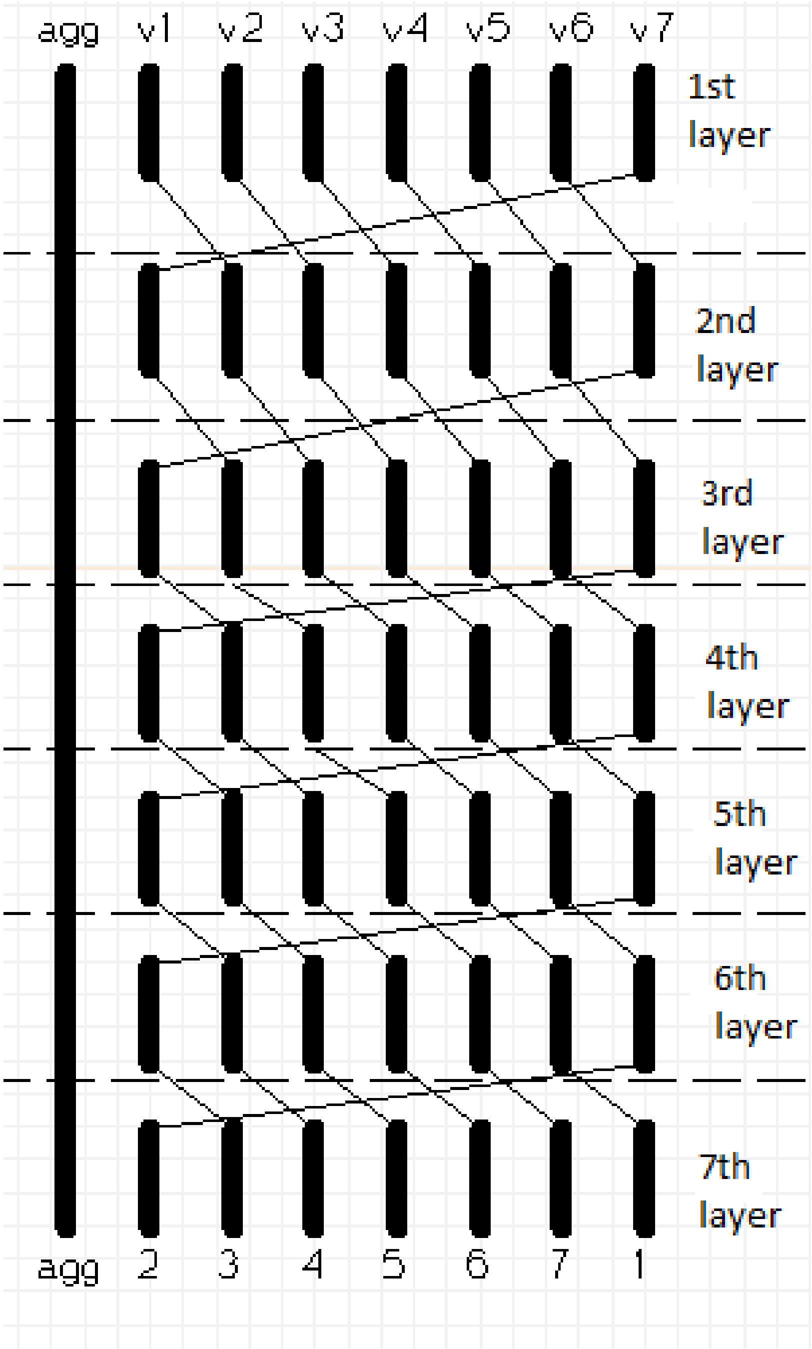
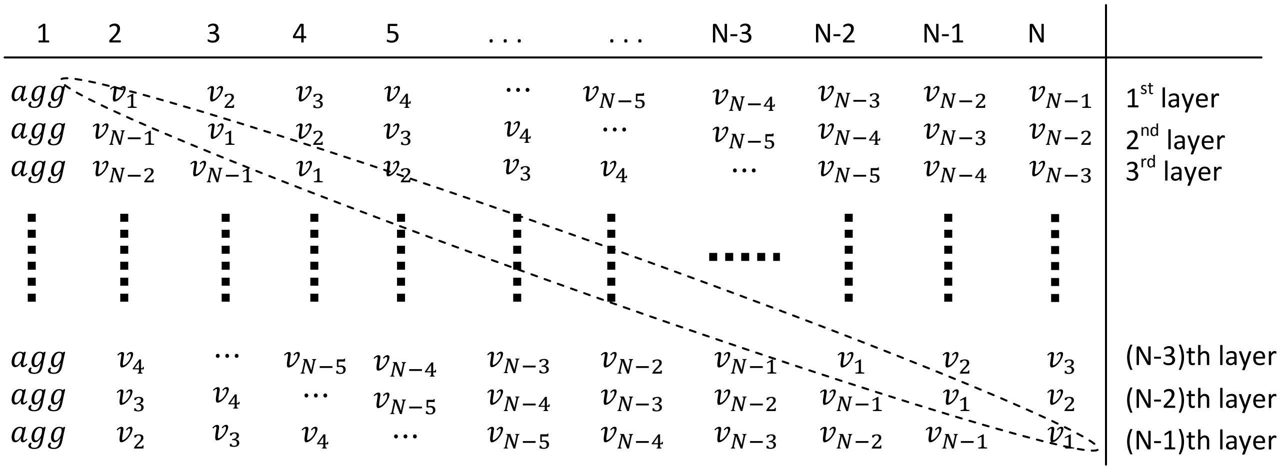


Figure 1.12. Optimal swizzling pattern of an eight bit TSV data bus.

1.5.3 Optimal swizzling of an N bit data bus

For an *N* bit data bus, the number of swizzling events is *N-2,* making each victim line adjacent to the aggressor line only once. The ideal case of a symmetric impedance distribution of a TSV data bus is to maintain the same impedance of each bit line. Based on this principle, all of the victim signal paths change directions during each swizzling event, as shown in Figure 1.13.



1	2	3	4	5	. . .	. . .	N-3	N-2	N-1	N	
agg	v_1	v_2	v_3	v_4	$\cdots$	v_{N-5}	v_{N-4}	v_{N-3}	v_{N-2}	v_{N-1}	1st layer
agg	v_{N-1}	v_1	v_2	v_3	v_4	$\cdots$	v_{N-5}	v_{N-4}	v_{N-3}	v_{N-2}	2nd layer
agg	v_{N-2}	v_{N-1}	v_1	v_2	v_3	v_4	$\cdots$	v_{N-5}	v_{N-4}	v_{N-3}	3rd layer
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋯	⋮	⋮	⋮	
agg	v_4	$\cdots$	v_{N-5}	v_{N-4}	v_{N-3}	v_{N-2}	v_{N-1}	v_1	v_2	v_3	(N-3)th layer
agg	v_3	v_4	$\cdots$	v_{N-5}	v_{N-4}	v_{N-3}	v_{N-2}	v_{N-1}	v_1	v_2	(N-2)th layer
agg	v_2	v_3	v_4	$\cdots$	v_{N-5}	v_{N-4}	v_{N-3}	v_{N-2}	v_{N-1}	v_1	(N-1)th layer

Figure 1.13. Optimal swizzling pattern of an N bit TSV data bus.

In the optimal swizzling pattern, each victim signal path passes through all of the physical positions in the data bus structure. For example, v_1 is propagated on the second bit line at the first layer and then swizzled to the third bit line at the second layer. The output signal v_1 appears at the N^{th} bit line at the $(N-1)^{th}$ layer. Other victim signal paths also abide with this principle, achieving a symmetric distribution of the coupling impedances.

1.5.4 Conclusions

The application of swizzling to a TSV data bus is constrained by the physical structure of the TSV. As the length of a TSV is dependent on the thickness of the substrate, it is not possible to change the direction of a signal path in the middle of a TSV but only at the end of the TSV. This property of discrete segments poses a limitation on swizzling in a 3-D system. However, an advantage of the optimal swizzling pattern is that this pattern is signal independent.

The proposed optimal swizzling pattern assumes that the edge line of a data bus is the aggressor line which propagates the fastest transition signal. As the least significant bit (LSB), which is the edge line of a data bus, generally exhibits the greatest switching, it is reasonable to assume the fastest transition signal propagated along the edge line. When the aggressor signal is propagated in a middle bit line, the bit lines of a data bus can be divided into two groups, with the aggressor line residing at the edge of each of the groups. The situation in each group becomes the same as the situation discussed in the previous section. The proposed optimal swizzling method is therefore treated as signal independent.

Chapter 2

A description of the simulations and theoretical analyses is provided in this chapter. Specifically, the HSPICE circuit models of a TSV data bus with different swizzling patterns are simulated and a MATLAB model is proposed. The closed-form expression of a newly defined coefficient is also discussed.

2.1 HSPICE simulation

In this section, the HSPICE circuit setup is illustrated, simulation results are presented, and some explanations are offered.

2.1.1 HSPICE circuit setup

A circuit model of two coupled TSVs is shown in Figure 2.1, which is the basic element of a TSV data bus simulated in HSPICE. There are five parameters: self-resistance R_{self}, self-inductance L_{self}, self-capacitance C_{self}, coupling capacitance $C_{coupling}$, and the mutual inductance represented by the inductive coupling coefficient k_i. Based on (1.1) - (1.14), the value of the parameters in a TSV data bus is listed in Table 2.1.

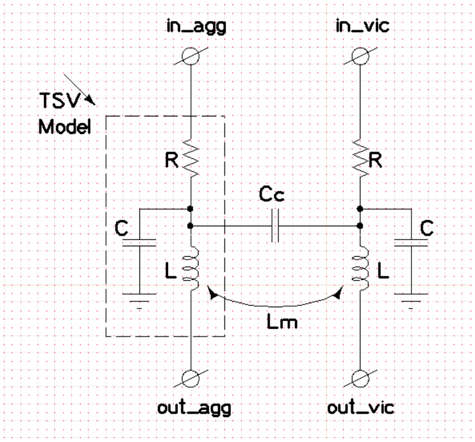


Figure 2.1. HSPICE circuit model of two coupled TSVs.

Table 2.1. Parameters of two coupled TSVs

AR	R	L_self (e-9)	C_self (e-12)	C_coupling (e-13)	$k1$	$k2$	$k3$	$k4$	$k5$	$k6$	$k7$
5	0.0367	0.021	0.1099	0.063	0.4196	0.3114	0.2466	0.2034	0.1728	0.15	0.1324
10	0.0735	0.055	0.1586	0.1335	0.5226	0.4124	0.341	0.2905	0.2527	0.2233	0.1998
15	0.1102	0.094	0.192	0.2079	0.5828	0.4746	0.4024	0.3497	0.3093	0.2771	0.2509
20	0.1469	0.1364	0.2119	0.2861	0.6244	0.5185	0.4467	0.3935	0.352	0.3186	0.2909
25	0.1836	0.1812	0.2167	0.3671	0.656	0.5521	0.4809	0.4277	0.3859	0.3518	0.3234
30	0.2204	0.2279	0.2028	0.4505	0.6812	0.5791	0.5087	0.4557	0.4138	0.3794	0.3506
35	0.2571	0.2763	0.1654	0.5358	0.7021	0.6015	0.5319	0.4792	0.4374	0.4029	0.3738
40	0.2938	0.3261	0.0982	0.6228	0.7199	0.6207	0.5518	0.4995	0.4577	0.4232	0.3941

$*\ ki\text{: } inductive\ coupling\ coefficient\ between\ two\ TSVs.$ $\quad *\ AR\text{: } aspect\ ratio = \frac{length}{diameter}.$

$*\ i\text{: } number\ of\ pitches\ between\ two\ TSVs.$ $\quad *\ TSV\ diameter = 10\ \mu\text{m}, barrier = 0.2\ \mu\text{m}.$

$*\ TSVs\ pitch = separation + 2(radius + barrier), separation = 10\ \mu\text{m}.$

2.1.2 HSPICE simulation results

The input of the aggressor line is a ramp signal, while the other victim lines are at ground. The reduction in peak coupling noise, as compared to the no swizzling case, is listed in Tables 2.2 and 2.3, where D is the TSV diameter of cross-section, AR is the TSV aspect ratio, which is TSV length over diameter, and TR is the transition time of the ramp signal on the aggressor line. P1, P2, and OP represent, respectively, swizzling pattern I, II, and the optimal pattern.

Table 2.2. Reduction in peak coupling noise as compared to no swizzling when TR is 10 ps

AR/D	1 um			5 um			10 um			20 um		
%	P1	P2	Op	P1	P2	Op	P1	P2	Op	P1	P2	Op
5	-0.8	45.0	51.4	13.4	7.8	-2.2	14.2	17.1	5.67	20.9	17.3	9.4
10	-3.1	-7.4	-4.8	3.5	15.8	4.5	12.1	32.7	13.6	18.6	36.6	26.1
15	-6.0	-1.6	0.34	2.8	18.9	23.3	7.0	25.4	27.5	13.7	26.8	11.8
20	0.0	4.9	4.9	2.8	16.0	27.1	7.2	21.6	23	9.6	18.5	25.3
25	-3.7	4.8	5.85	-10.9	7.3	17.7	7.5	17.9	21.6	7.2	13.7	20.9
30	-11.1	-3.0	-1.0	-18.2	0.0	9.0	0.8	10.5	18.5	4.5	11.2	19.4
35	-14.3	-6.7	4.3	-38.1	-15.1	-0.48	-10.5	-1.8	12.6	-4.0	3.2	15.1
40	-30.4	-17.8	-5.2	-57.5	-35.2	-16.9	-44.6	-29.1	-12.6	-21.1	-7.3	7.3
AR/D	30 um			40 um			50 um			60 um		
%	P1	P2	Op	P1	P2	OP	Op	P2	OP	P1	P2	Op
5	21.8	23.8	17.7	23.8	28.5	19.2	21.6	24.8	21.2	20.8	24.0	15.7
10	17.9	34.6	19.8	17.2	33.1	19.6	17.5	33.1	21.1	17.4	33.5	21.7
15	14.0	24.8	29.9	14.4	25.6	34.4	14.3	24.8	21.1	15.4	25.3	20.5
20	10.7	18.1	26.2	13.7	20.3	26.8	13.1	20.3	15.8	14.2	21.3	22.2
25	11.1	16.7	20.8	11.0	16.6	31.0	11.0	16.4	18.4	11.6	17.0	16.4
30	7.3	11.7	19	8.6	11.5	27.3	9.9	12.7	16.9	9.9	12.0	15.5
35	0.8	6.8	20	2.2	7.5	23.1	2.9	8.8	18.4	2.2	7.4	18.4
40	-17.1	-4.7	13.23	-11.9	-2.2	16.3	-10.9	-2.2	13.1	-17.4	-7.6	11.7
AR/D	70 um			80 um			90 um			100 um		
%	P1	P2	Op	P1	P2	Op	P1	P2	Op	P1	P2	Op
5	23.2	23.9	14.9	23.1	23.7	15.5	23.4	28.5	15.4	21.6	24.8	15.8
10	17.4	32.9	24.6	17.3	33.3	25.7	16.8	32.9	26.8	17.5	33.1	26.9
15	14.2	25.3	21	14.1	25.8	32.1	14.1	25.2	31.3	14.3	24.8	31.3
20	13.5	20.6	22.6	13.0	20.1	22.6	13.5	20.5	21.4	13.1	20.3	21.8
25	12.1	16.8	17	10.8	15.5	16.8	10.8	15.5	17	11.0	16.4	16.9
30	9.2	12.0	15.5	7.7	12.0	15.5	7.7	12.6	16.2	9.9	12.7	17.5
35	1.5	6.6	19.1	4.2	9.1	20.4	6.0	10.7	23.8	2.9	8.8	25.5
40	-23.0	-14.3	6.8	-34.7	-22.0	0.8	-38.8	-25.0	-7.6	-10.9	-2.2	-10.3

The reduction in peak coupling noise of a swizzled data bus as compared to the no swizzling case for different TSV diameters is shown in Figure 2.2. When the TSV diameter is smaller than 5 µm, the efficiency of swizzling fluctuates. For example, for the 1 μm case, when the aspect ratio is five, pattern II achieves a 45% reduction as compared to no swizzling but falls to -7.4% when the aspect ratio is ten. This fluctuation can be explained based on the TSV impedances. When the TSV diameter is small, such as 1 μm, the self-resistance is large. A small current induced by the effect of capacitive coupling can therefore produce a noticeable noise on the victim line. Based on (1.1), the self-resistance grows with increasing aspect ratio, suggesting that a greater noise can be produced. The efficiency of swizzling however does not increase in the same manner as the noise amplitude. This mismatch causes uncertainty in reducing the peak coupling noise. When the TSV diameter is larger than 5 μm, the reduction follows a trend described by the dashed curve shown in Figure 2.2. The efficiency of swizzling increases to the maximum when the aspect ratio is ten and decreases with increasing aspect ratio.

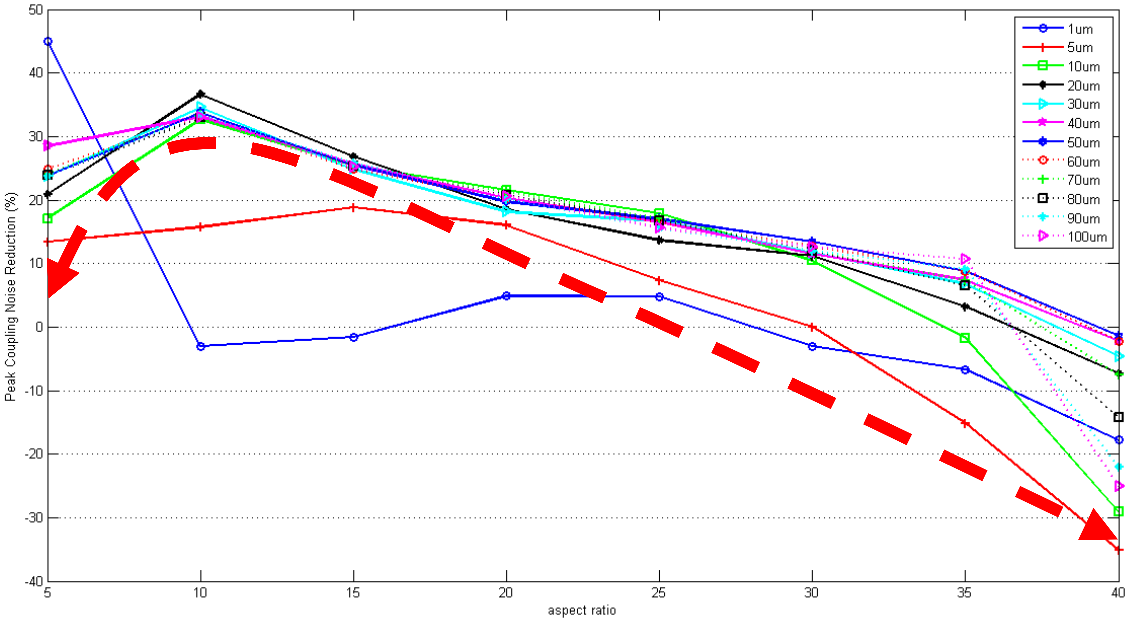


Figure 2.2. Reduction in peak coupling noise with respect to TSV aspect ratio (pattern II).

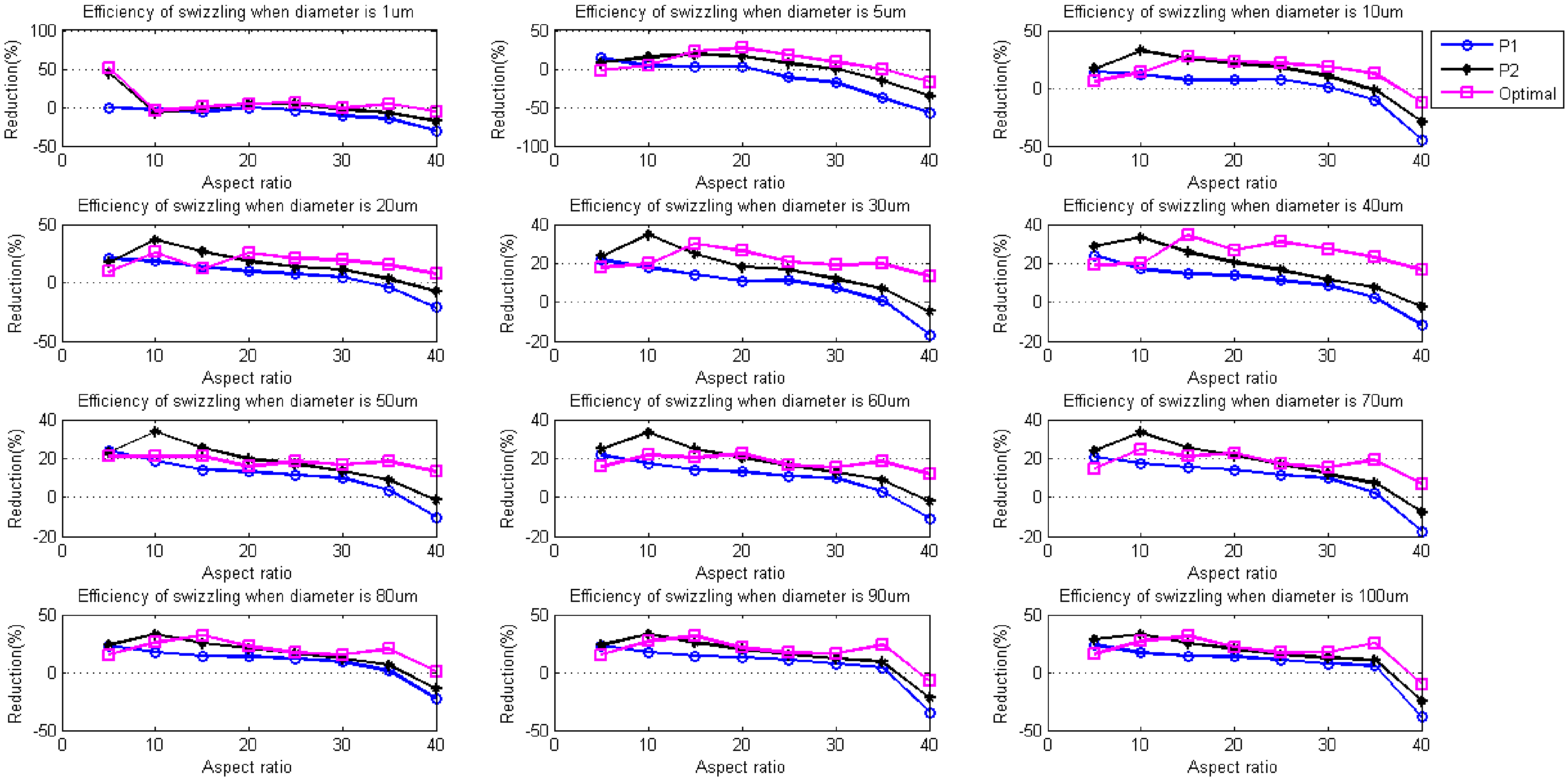


Figure 2.3. Comparison of efficiency of the three swizzling patterns.

The efficiency of the swizzling patterns is compared in Figure 2.3. The priority of the optimal pattern can be observed when the TSV aspect ratio is larger than 15.

The reduction in peak coupling noise of a swizzled data bus as compared to the no swizzling case for different transition times is shown in Figure 2.4. The reduction follows a trend described by the dashed curve, which illustrates that the efficiency of swizzling decreases with increasing transition time. When the aspect ratio is smaller than 15, the data do not completely agree with this trend. However, a decreasing trend can be observed when the transition time is smaller than 60 ps. Swizzling is therefore shown to be more efficient in reducing peak coupling noise when the transition of the ramp signal along the aggressor line is faster, as supported by HSPICE simulation.

Table 2.3. Reduction in peak coupling noise as compared to no swizzling when D is 10 μm

TR/AR	5			10			15			20		
%	P1	P2	OP	P1	P2	OP	P1	P2	OP	P1	P2	OP
10 ps	14	17	6	12	33	14	7	25	27	7	22	23
20 ps	14	10	-5	12	24	6	7	24	22	8	21	22
30 ps	-5	4	-12	13	19	-4	9	17	11	6	19	25
40 ps	12	16	19	11	14	-8	8	13	2	3	11	15
50 ps	10	5	-10	6	6	-17	8	10	-3	6	9	8
60 ps	1	-7	-39	3	-2	-13	2	4	-9	5	5	4
70 ps	-11	1	-21	7	9	6	-12	-13	-20	-4	-3	1
80 ps	-20	-4	-6	21	27	32	-12	-11	-14	-13	-12	-5
90 ps	26	20	20	13	18	18	-6	-5	2	-21	-20	-12
100 ps	24	26	0	20	20	11	-2	1	13	-14	-13	-2
TR/AR	25			30			35			40		
%	P1	P2	OP	P1	P2	OP	P1	P2	OP	P1	P2	OP
10 ps	7	18	22	1	10	19	-11	-2	13	-45	-29	-13
20 ps	0	14	17	-4	10	15	-10	4	10	-48	-26	-17
30 ps	1	14	20	-3	10	17	-16	0	7	-57	-38	-19
40 ps	-2	9	18	-6	5	15	-21	-7	5	-61	-45	-23
50 ps	1	5	10	-7	-1	13	-21	-12	5	-59	-48	-28
60 ps	1	2	2	-6	-2	5	-11	-6	2	-50	-48	-31
70 ps	-1	1	5	1	-1	7	-5	-7	0	-47	-48	-37
80 ps	-15	-14	-6	-13	-11	-2	-10	-8	-2	-48	-56	-41
90 ps	-25	-22	-12	-21	-16	-4	-23	-19	-8	-50	-59	-37
100 ps	-27	-24	-9	-31	-28	-9	-33	-33	-13	-49	-58	-30

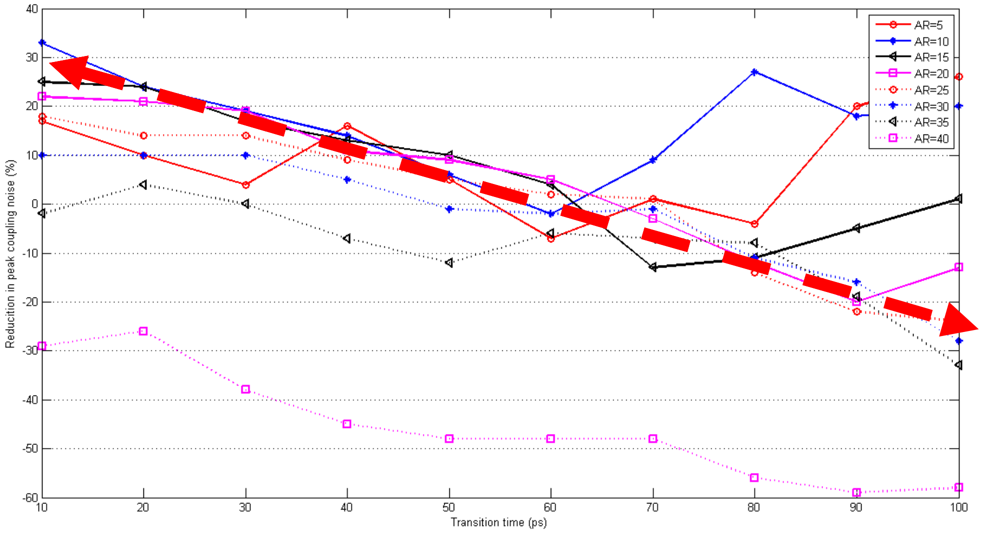


Figure 2.4. Reduction in peak coupling noise as compared to no swizzling when D is 10 μm.

2.1.3 Conclusions and analyses

In this section, four important conclusions are extracted from the circuit analyses, and corresponding explanations are provided.

Conclusion I: when the aspect ratio of a TSV is small, swizzling is more efficient. Swizzling distributes the noise of an aggressor to each line within a data bus. This distributive process reduces the peak coupling noise but also produces noise on the more distant victim lines. When the amplitude of the noise is sufficiently large, each bit line of a TSV data bus can operate as both an aggressor and a victim. The peak coupling noises induced by all of the aggressors can accumulate on a middle victim line. As the induced noise is due to coupling, if the coupling is sufficiently significant, the accumulated noise will exceed the no swizzling case. As shown by the data listed in Table 2.1, when the TSV aspect ratio increases, the mutual coupling parameters also increase. Coupling between the TSV bit lines can become sufficiently significant to cancel the advantages of swizzling. Therefore, swizzling is more likely to exhibit greater utility in a TSV data bus with a smaller TSV aspect ratio.

Conclusion II: in the non-swizzling case, the peak coupling noise can appear on the farthest victim line. Each bit line of a TSV data bus acts as both an aggressor and a victim. Although the peak noise should appear on the middle victim line rather than an edge line, as shown in Figure 1.1, when the noises on two adjacent lines switch in opposite directions, the crosstalk noise can be reduced to zero [18]. Another reason is that the victim line itself can also produce noise. When the frequency of the propagated signal is comparable to the resonance frequency of this equivalent noise generator [1], the noise amplitude can become significant without the influence of the aggressor.

Conclusion III: the peak coupling noise appears on a bit line that exhibits the largest parasitic impedance. Based on HSPICE simulations and (1.15) - (1.17), for pattern I, the peak noise appears at the output of v_1; for pattern II, the peak noise appears at the output of v_2; for the optimal pattern, the peak noise randomly appears at any victim signal path. This result operates for all transition times and diameters. To explain this behavior, the impedance of each decoupled data path within the bus needs to be determined. Based on the results described in Appendix A, the inductance of the victim signal path, which produces the greatest peak noise, is expressed as (1.17) - (1.21).

For no swizzling,

$$L_{max\_noswizzling} = L_{vic1} = 7(L_{self} + L_{m2} + L_{m3} + L_{m4} + L_{m5} + L_{m6}), \quad (1.17)$$

for pattern I:

$$L_{max\ \_P1} = L_{vic1} = 7L_{self} + L_{m2} + 7L_{m3} + 7L_{m4} + 7L_{m5} + L_{m6}, \quad (1.18)$$

for pattern II:

$$L_{vic2} = 7L_{self} + L_{m3} + L_{m4} + L_{m5}, \quad (1.19)$$

$$L_{max\ \_P2} = L_{vic3} = 7L_{self} + L_{m2} + L_{m3} + 3L_{m4} + L_{m5} + L_{m6}, \quad (1.20)$$

and for the optimal pattern:

$$L_{max\ \_op} = 7L_{self} - L_{m7} - L_{m6} - L_{m5} - L_{m4} - L_{m3} - L_{m2} - L_{m1}. \quad (1.21)$$

The maximum inductance of each swizzling pattern is smaller than the non-swizzling pattern and, among the three swizzling patterns, $L_{max\ \_op}$ is the smallest. As the impedance is determined by the resistance, inductance, and capacitance, while the capacitance of each victim signal path after decoupling is the same, the maximum impedance of the optimal pattern is smaller than any other patterns. The optimal swizzling pattern therefore lowers the peak coupling noise, which is illustrated in Figure 2.3. The assumption that the higher impedance of a decoupled signal path, the larger the peak coupling noise, is therefore demonstrated. Although in swizzling pattern II, the peak coupling noise appears on v_2 while v_3 has the maximum impedance, this behavior supports this assumption due to the dual attribute of each line as an aggressor and a victim.

Conclusion IV: when the ramp signal transition on the aggressor line is faster, swizzling is more efficient. If the voltage level of the signal propagated along an aggressor line switches from low to high, the electrical field in the coupling capacitor and the magnetic field surrounding the aggressor line become greater. The switching behavior of the signal on the aggressor produces a current through the coupling capacitance to the victim line. This switching behavior also changes the magnetic field surrounding the adjacent victim bit line.

Lenz's law states that an induced voltage tends to produce a current that flows in the direction that produces a flux that opposes the original change of flux [58]. The *Right Hand Rule* is described as, in a straight wire, the thumb of the right hand points to the direction of current, and the fingers point in the direction of the magnetic lines [59]. As shown in Figure 2.5, according to the Lenz's law and the right hand rule, the induced current on the victim line passes in the same direction as the aggressor signal. Hence, the inductive coupling increases the amplitude of the crosstalk noise on the victim line.

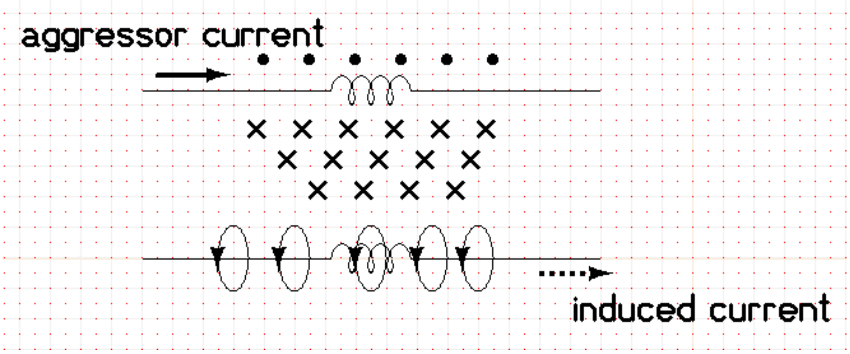


Figure 2.5. Induced current due to inductive coupling.

Both the induced capacitive current and inductive voltage exhibits a positively linear relationship with the speed of the transition. The faster the aggressor signal switches, the larger the peak coupling noise on the victim line.

As shown in Figure 2.1, a T-type RLC model of a TSV is assumed. For each bit line of a TSV data bus, the HSPICE circuit model is considered as a series of T-type RLC filters, as illustrated in Figure 2.6.

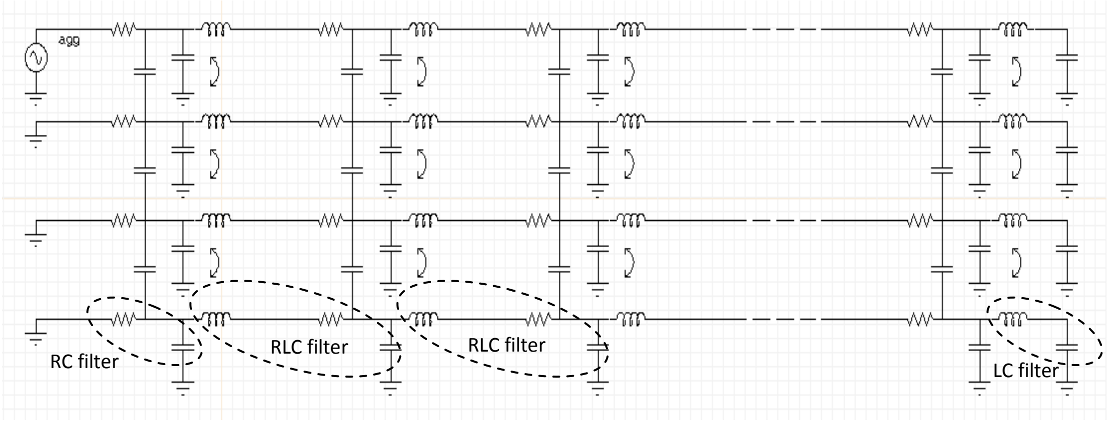


Figure 2.6. HSPICE model of a four bit TSV data bus.

After decoupling, each bit line behaves as an RC filter at the input end, several RLC filters in the middle, and a LC_{load} filter at the output end. The transfer function of each filter, according to Kirchoff's circuit law [60], is

$$N(\omega)_{RC} = \frac{1}{1+j\omega RC}, \tag{1.22}$$

$$N(\omega)_{LC} = \frac{1}{1-\omega^2 LC}, \tag{1.23}$$

$$N(\omega)_{RLC} = \frac{1}{(1-\omega^2 LC)+j\omega RC}. \tag{1.24}$$

From Table 2.1, the inductance L of a TSV is on the order of 10^{-10} H while the capacitance C is on the order of 10^{-12} F. A modern integrated system can operate at gigahertz clock frequencies [61], which means the angular frequency ω is on the order of 10^9 Hz. The value of $\omega^2 LC$ is therefore dimensionless and on the order of 10^{-4} units. The effect of the inductance in a RLC and a LC filter can therefore be neglected within a TSV data bus, and the entire bit line can be considered as a series of low pass RC filters, where the cutoff angular frequency ω_c of each filter is $\frac{1}{\sqrt{RC}}$. When the signal along an aggressor switches faster, based on (1.1) and (1.6), R and C do not change, meaning the same low pass window will operate properly.

Analyzing the frequency domain of a ramp signal through a Fourier transformation, a faster switching signal contains more high frequency elements [62], [63]. Intuitively, a ramp signal with a 10 ps transition time can be transformed from a signal with a 100 ps transition time by adding more high frequency elements, as shown in Figure 2.7.

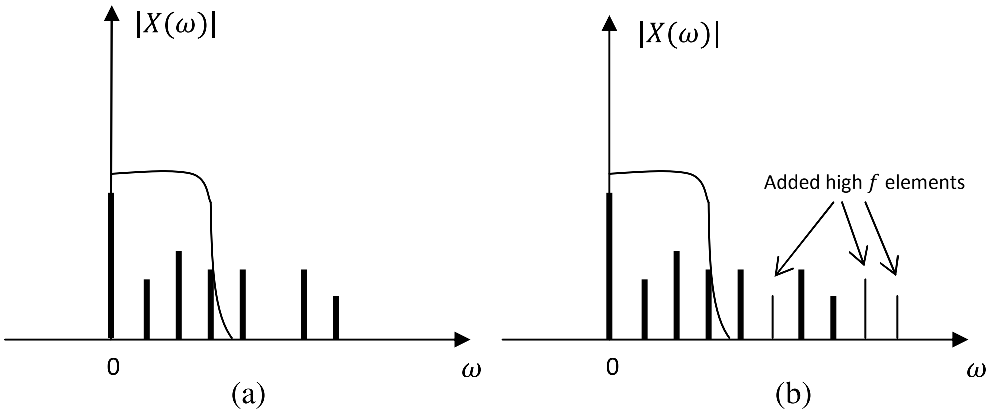


Figure 2.7: Filtering process for different transition times, a) 100 ps, and b) 10 ps.

As shown in Figure 2.7, the frequency elements inside the low pass window are the same within different transition times. The filtered outputs within different transition times are therefore the same. Assume the amplitude of the induced noise is N_{100ps} when the transition time is 100 ps, while the amplitude is N_{10ps} when the transition time is 10 ps. As the amplitude of the induced coupling noise is linear with the transition speed of the aggressor signal, N_{100ps} is smaller than N_{10ps}. Assume the amplitude of the output noise for these two cases is N_{output}. The reduction in peak coupling noise can be expressed as (1.25)

$$\frac{N_{10ps}-N_{output}}{N_{10ps}} > \frac{N_{100ps}-N_{output}}{N_{100ps}}, \tag{1.25}$$

demonstrating the assumption that swizzling is more efficient in reducing peak coupling noise when the signal along an aggressor line switches faster.

2.1.4 Summary

The efficiency of the swizzling patterns in reducing peak coupling noise is summarized in Table 2.4 based on the HSPICE simulations. D is the TSV diameter and AR is the TSV aspect ratio. The transition time of the aggressor signal is 10 ps. P1 is swizzling pattern I, P2 is swizzling pattern II, OP is the optimal swizzling pattern, and “no” represents no swizzling. Table 2.4 can be referred to when selecting the appropriate swizzling pattern for different TSV diameters and aspect ratios.

Table 2.4. Swizzling pattern for different TSV diameters and aspect ratios

TSV	D(μm)/AR	5	10	15	20	25	30	35	40
Thin	1	OP	NO	OP	P2/OP	OP	NO	NO	NO
	5	P1	P2	OP	OP	OP	OP	NO	NO
Bulk	10	P2	P2	OP	OP	OP	OP	OP	NO
	20	P1	P2	P2	OP	OP	OP	OP	OP
	30	P2	P2	OP	OP	OP	OP	OP	OP
	40	P2	P2	OP	OP	OP	OP	OP	OP
	50	P2	P2	P2	P2	OP	OP	OP	OP
	60	P2	P2	P2	P2	OP	OP	OP	OP
	70	P2	P2	P2	OP	P2/OP	OP	OP	OP
	80	P2	P2	P2	OP	OP	OP	OP	OP
	90	P2	P2	OP	OP	OP	OP	OP	NO
	100	P2	P2	OP	OP	OP	OP	OP	NO

2.2 MATLAB Modeling

As illustrated in Section 2.1.3, the efficiency of swizzling is dependent on the TSV diameter, aspect ratio, and switching speed of the signal along an aggressor line. The relationship between swizzling and TSV pitch also needs to be explored.

2.2.1 MATLAB Model

As MATLAB can be used to transform a physical structure to a mathematical expression [64], an equivalent MATLAB model describing the coupling effects in a 3-D IC TSV-based data bus is developed. Two variables, α and β, are defined to describe the inductive and capacitive coupling within a TSV data bus.

2.2.1.1 **Inductive coupling**

A normalized inductive coupling coefficient of two coupled TSVs is proposed as α. As a criterion of the level of inductive coupling, this coefficient is dependent on the distance between two TSV bit lines. As α is normalized from the physical inductive coupling parameter k_i, the derivation of α is also based on k_i,

$$k_i = \frac{L_m(i)}{\sqrt{L_1 \cdot L_2}} = \frac{L_m(i)}{L_{self}} \ , \tag{2.1}$$

where i is the distance (in terms of the number of pitches) between two TSVs. L_m is the mutual inductance and L_{self} is the self-inductance. A function $f_{ind}(i)$ represents the relation between $\frac{ki}{k1}$ and i,

$$f_{ind}(i) = \frac{ki}{k1} = \frac{L_m(i)}{L_m(1)}. \tag{2.2}$$

An expression of the mutual inductance is provided in (1.4) and (1.5). When the TSV pitch is P_0, the distance between any two TSV bit lines is $P = i \cdot P_0$. $f_{ind}(i)$ can therefore be expressed as

$$f_{ind}(i) = \frac{\ln\left(\frac{L+\sqrt{L^2+i^2{P_0}^2}}{i \cdot P_0}\right)L + i \cdot P_0 - \sqrt{L^2+i^2{P_0}^2}}{\ln\left(\frac{L+\sqrt{L^2+{P_0}^2}}{P_0}\right)L + P_0 - \sqrt{L^2+{P_0}^2}} \ . \tag{2.3}$$

As $L = D \cdot AR,\ f_{ind}(i)$ is transformed into a function of D, AR, P_0, and i,

$$f_{ind}(D, AR, P_0, i) = \frac{\ln\left(\frac{D \cdot AR+\sqrt{D^2AR^2+i^2{P_0}^2}}{i \cdot P_0}\right) \cdot D \cdot AR + i \cdot P_0 - \sqrt{D^2AR^2+i^2{P_0}^2}}{\ln\left(\frac{D \cdot AR+\sqrt{D^2AR^2+{P_0}^2}}{P_0}\right) \cdot D \cdot AR + P_0 - \sqrt{D^2AR^2+{P_0}^2}} \ . \tag{2.4}$$

The normalized inductive coupling coefficient of any two TSVs can be expressed as

$$\alpha(D, AR, P_0, i) = \alpha_0 * f_{ind}(D, AR, P_0, i), \tag{2.5}$$

where α_0 is the initial value of the normalized inductive coupling coefficient when the distance between two bit lines is one pitch. The diameter, aspect ratio, and transition time of the signal along an aggressor line are assumed to be known. The effect of adjacent and non-adjacent inductive coupling in a TSV data bus is illustrated in Figure 2.8.

N_{ji} is the peak noise of the i^{th} bit line on the j^{th} layer induced by the inductive coupling,

$$\begin{aligned}
N_{(j+1)1} &= N_{(j+1)0} \cdot \alpha(1) + N_{j2} \cdot \alpha(1) + N_{j3} \cdot \alpha(2) + N_{j4} \cdot \alpha(3) \\
&\qquad + N_{j5} \cdot \alpha(4) + N_{j6} \cdot \alpha(5) + N_{j7} \cdot \alpha(6)\ ; \\
N_{(j+1)2} &= N_{(j+1)1} \cdot \alpha(1) + N_{j3} \cdot \alpha(1) + N_{j4} \cdot \alpha(2) + N_{j5} \cdot \alpha(3) \\
&\qquad + N_{j6} \cdot \alpha(4) + N_{j7} \cdot \alpha(5); \\
N_{(j+1)3} &= N_{(j+1)2} \cdot \alpha(1) + N_{j4} \cdot \alpha(1) + N_{j5} \cdot \alpha(2) + N_{j6} \cdot \alpha(3) + N_{j7} \cdot \alpha(4); \\
N_{(j+1)4} &= N_{(j+1)3} \cdot \alpha(1) + N_{j5} \cdot \alpha(1) + N_{j6} \cdot \alpha(2) + N_{j7} \cdot \alpha(3); \\
N_{(j+1)5} &= N_{(j+1)4} \cdot \alpha(1) + N_{j6} \cdot \alpha(1) + N_{j7} \cdot \alpha(2); \\
N_{(j+1)6} &= N_{(j+1)5} \cdot \alpha(1) + N_{j7} \cdot \alpha(1); \\
N_{(j+1)7} &= N_{(j+1)6} \cdot \alpha(1).
\end{aligned}$$

2.2.1.2 Capacitive coupling

A normalized capacitive coupling coefficient of two adjacent TSVs is proposed as β. This coefficient represents the capacitive coupling between a pair of adjacent TSVs. The capacitive coupling between two non-adjacent TSV bit lines is neglected [65].

Based on the expression of the coupling capacitance between two adjacent TSV bit lines in (1.11), a function $f_{cap}(AR)$ represents $\frac{C_{coupling}(AR)}{C_{coupling}(AR=5)}$ with respect to the aspect ratio of a TSV,

$$f_{cap}(AR) = \frac{AR \cdot [0.225 \cdot \ln(0.97 \cdot AR) + 0.53][1.315 \cdot AR^{-0.988} + 0.85 - e^{-AR+1.3}]}{4.8398}. \tag{2.6}$$

The normalized capacitive coupling coefficient of any two coupled TSV bit lines is

$$\beta(AR) = \beta_0 * f_{cap}(AR), \tag{2.7}$$

where β_0 is the initial value of the normalized capacitive coupling coefficient. Based on the decoupling technique described in Chapter 1.4.3, the capacitance of each bit line of a TSV data bus, after decoupling, is similar while the inductance tends to be quite different, which means that the mutual inductance is the primary factor that determines the parasitic impedance. β_0 is, therefore, assumed to be constant. The effect of capacitive coupling in a TSV data bus is illustrated in Figure 2.9.

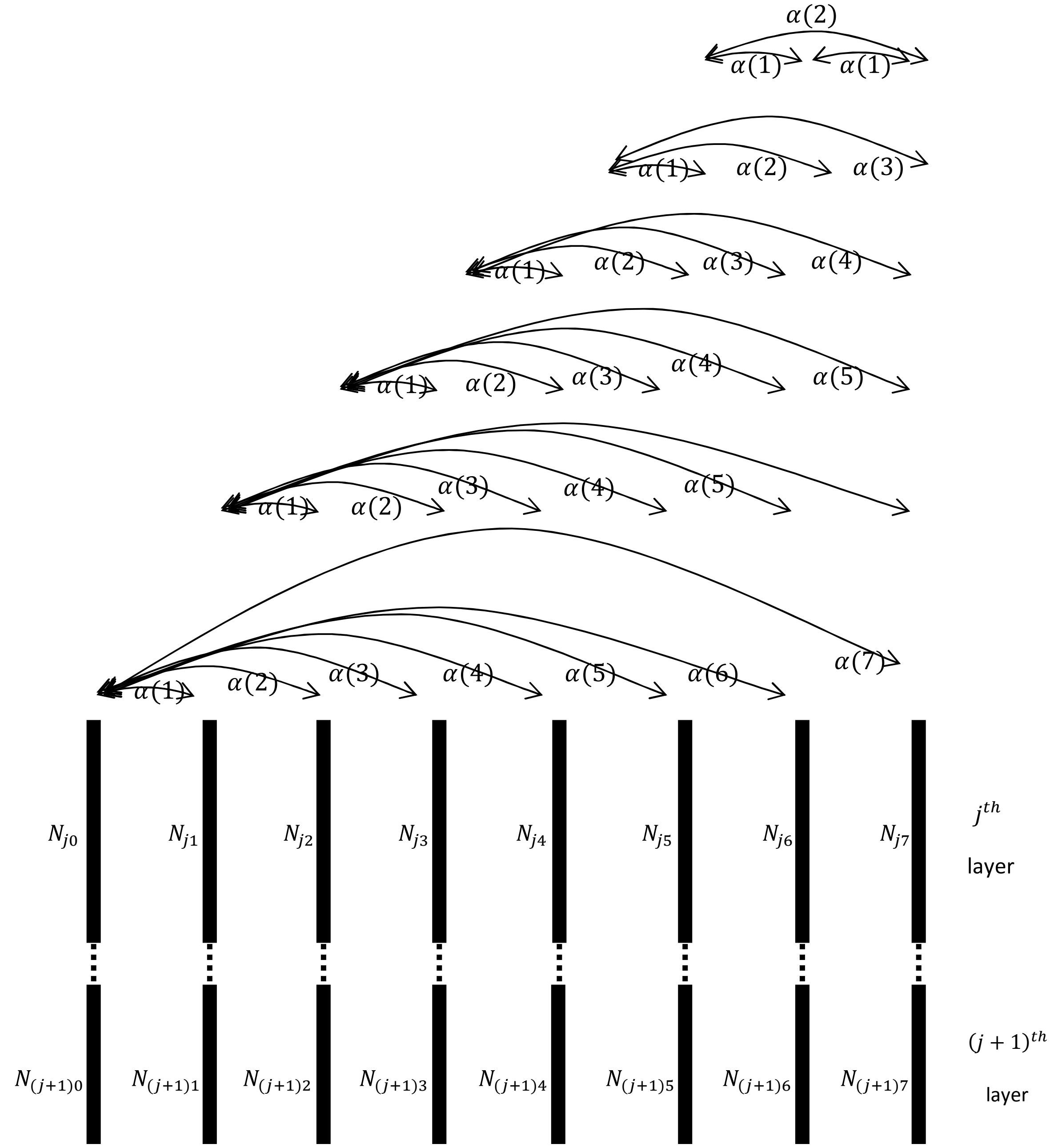


Figure 2.8. Inductive coupling within a TSV data bus, where $\alpha(i)$ is the normalized inductive coupling coefficient and i is the distance (in terms of the number of pitches) between two bit lines.

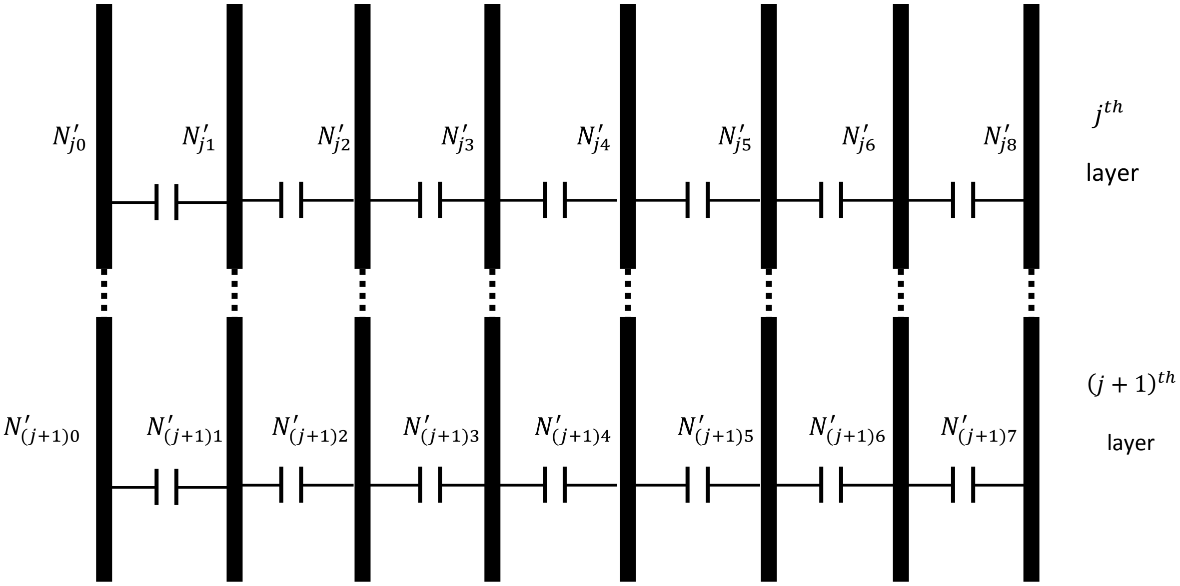


Figure 2.9. Capacitive coupling within a TSV data bus.

N'_{ji} is the peak noise of the i^{th} bit line on the j^{th} layer induced by the capacitive coupling.

$$N'_{(j+1)1} = N'_{(j+1)0} \cdot \beta + N'_{j2} \cdot \beta;$$

$$N'_{(j+1)2} = N'_{(j+1)1} \cdot \beta + N'_{j3} \cdot \beta;$$

$$N'_{(j+1)3} = N'_{(j+1)2} \cdot \beta + N'_{j4} \cdot \beta;$$

$$N'_{(j+1)4} = N'_{(j+1)3} \cdot \beta + N'_{j5} \cdot \beta;$$

$$N'_{(j+1)5} = N'_{(j+1)4} \cdot \beta + N'_{j6} \cdot \beta;$$

$$N'_{(j+1)6} = N'_{(j+1)5} \cdot \beta + N'_{j7} \cdot \beta;$$

$$N'_{(j+1)7} = N'_{(j+1)6} \cdot \beta.$$

2.2.2 Additive property of coupling coefficients

Capacitive coupling produces a current on a victim line through the coupling capacitor while the inductive coupling induces a voltage on the victim line through the mutual inductor. As both inductive and capacitive coupling results in coupling noise, the corresponding voltages can be summed. Therefore, for the worst case where the noise exhibits the same phase, the peak coupling noise of the i^{th} bit line on the j^{th} layer is the summation of the induced inductive noise N_{ji} and the capacitive noise N'_{ji}. A new coefficient γ, which is the summation of α and β, can therefore be proposed to describe the worst case coupling within a TSV data bus with respect to the TSV diameter D, pitch P, distance $i \cdot P$, and aspect ratio AR,

$$\gamma = \begin{cases} \alpha(D,P,i,AR) + \beta(AR), i = 1 \\ \alpha(i,AR,D,P), \qquad\qquad i > 1 \end{cases} \tag{2.8}$$

where the effect of capacitive coupling is neglected when the TSV separation is greater than a pitch. According to the differential expression of a current through a capacitor and a voltage across an inductor in, respectively, (2.9) and (2.10),

$$i_{cap} = C\frac{dv}{dt} \ , \tag{2.9}$$

$$v_{ind} = L\frac{di}{dt} \ , \tag{2.10}$$

the faster the signal along an aggressor line switches, the larger the peak coupling noise induced on the victim line. An expression of the worst case peak noise including capacitive and inductive coupling is therefore

$$N_{peak} = R_{self} * i_{cap} + v_{ind}. \tag{2.11}$$

2.2.3 MATLAB simulation results

The reduction in peak coupling noise versus α_0 for different aspect ratios is shown in Figure 2.10. A nonlinear relationship between the efficiency of swizzling and α_0 is illustrated in Figure 2.11. Two boundary points, A and B, divide the entire range of α_0 into three parts. The $swizzling\ efficient\ zone$ is the range of α_0 where a lower peak coupling noise is induced on the victim line by a swizzled TSV data bus. The $no\ swizzling\ efficient\ zone$ is the range of α_0 where a lower peak coupling noise is induced on the victim line by a non-swizzled TSV data bus. Only when α_0 ranges between A and B can the efficiency of swizzling be guaranteed. The boundary values of α_0, for different TSV aspect ratios, are listed in Table 2.5.

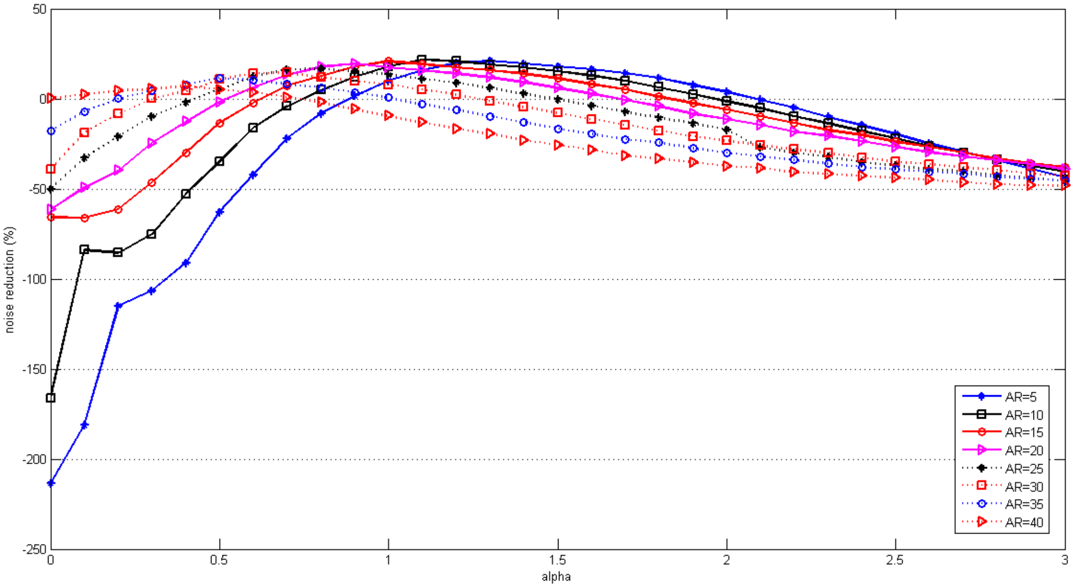


Figure 2.10. Reduction in peak coupling noise with respect to α_0.

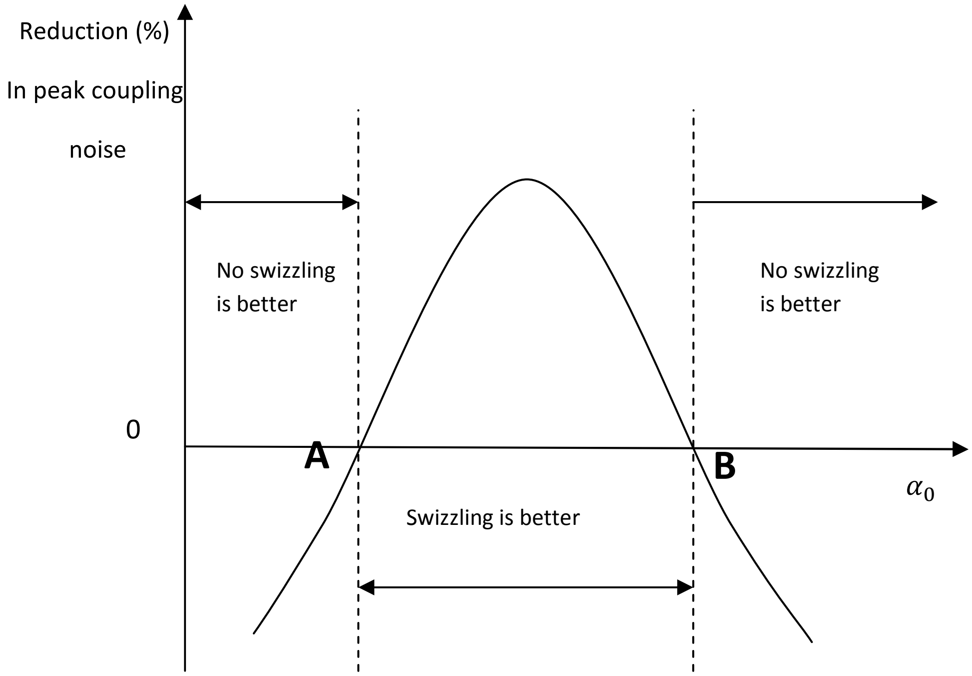


Figure 2.11. Swizzling efficient zone and no swizzling efficient zones.

Table 2.5 Value of boundary A and B

Aspect Ratio/α_0	No swizzling Efficient Zone(≤ A)	Swizzling Efficient Zone			No swizzling Efficient Zone(≥ B)
5	0.9~1	Pattern I Efficient Zone	1.5~1.6	Pattern II Efficient Zone	2~2.1
10	0.8		1.3~1.4		1.9~2
15	0.7		1.2~1.3		1.8~1.9
20	0.6		1.1~1.2		1.6~1.7
25	0.5		0.9~1		1.4~1.5
30	0.3~0.4		0.8~0.9		1.2~1.3
35	0.2~0.3		0.6~0.7		0.9~1
40	0.1~0.2	PatternII Efficient Zone			0.7~0.8

The initial value α_0 of the normalized inductive coupling coefficient is obtained based on the mutual inductive coefficient k_1, as listed in Table 2.1. These two parameters are similarly dependent on the impedance parameters of a TSV data bus.

From a physical point of view, k_1, representing the inductive coupling level between two adjacent TSV bit lines, is determined by the TSV pitch. The efficiency of swizzling when the TSV diameter is 10 µm and the transition time of an aggressor signal is 10 ps, for different TSV pitch cases, is shown in Table 2.6 and Figure 2.12.

When the value of k_1 or α_0 is relatively small, meaning the distance between two adjacent TSVs is large, the inductive coupling is negligible and the signal integrity along a non-swizzled TSV data bus is not affected. In this case, applying swizzling can degrade the performance of a data bus. Alternatively, when the inductive coupling is significant, namely k_1 or α_0 is large, the advantages of swizzling can be canceled since each bit line behaves as an aggressor and a victim, as explaned in Chapter 2.1.3. Only when the inductive coupling is in the swizzling efficient zone can swizzling minimize the peak coupling noise. Therefore, swizzling is a *conditionally* efficient method in reducing peak coupling noise in a TSV data bus.

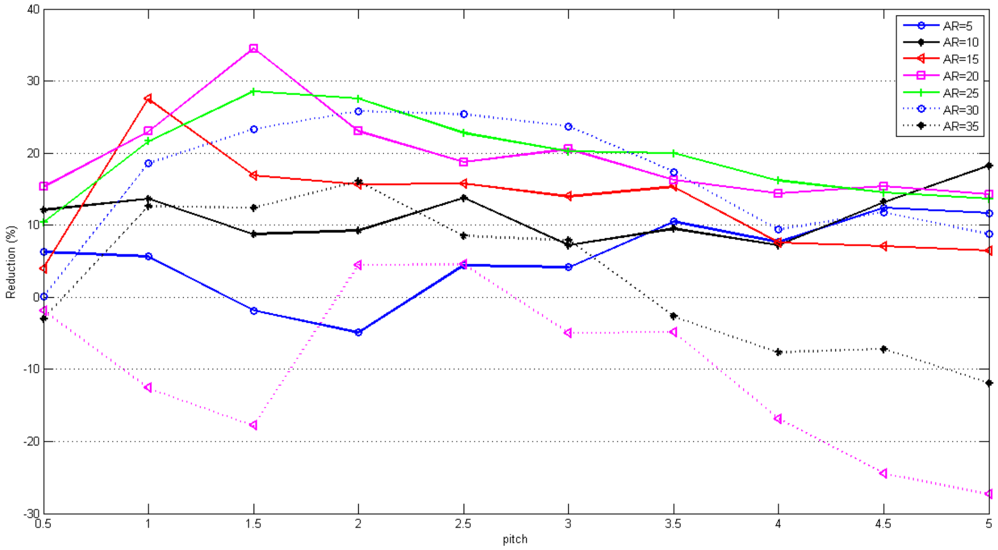


Figure 2.12. Reduction in peak coupling noise as a fuction of TSV pitch.

Table 2.6 Reduction in peak coupling noise for different TSV pitches

Pitch/AR	5	10	15	20	25	30	35	40
0.5	6.25	12.10	4.00	15.30	10.37	0.10	-2.97	-1.89
1	5.65	13.64	27.46	23.02	21.64	18.55	12.63	-12.60
1.5	-1.86	8.73	16.90	34.51	28.57	23.31	12.40	-17.83
2	-4.90	9.24	15.67	23.02	27.57	25.85	16.07	4.46
2.5	4.43	13.79	15.75	18.75	22.79	25.41	8.50	4.55
3	4.18	7.21	13.95	20.56	20.25	23.71	7.91	-4.95
3.5	10.48	9.53	15.32	16.26	20.00	17.36	-2.64	-4.85
4	7.65	7.23	7.56	14.41	16.17	9.35	-7.63	-16.90
4.5	12.41	13.24	7.08	15.38	14.52	11.82	-7.22	-24.43
5	11.70	18.22	6.48	14.29	13.68	8.77	-11.90	-27.36

2.3 HSPICE and MATLAB simulations

Factors that affect the efficiency of swizzling in a 3-D TSV data bus include the TSV diameter, aspect ratio, pitch, and switching speed of the signal along an aggressor line. The relationship between the efficiency of swizzling and TSV diameter, aspect ratio, and switching speed has been evaluated by HSPICE simulations (see Chapter 2.1). The effect of the TSV pitch on swizzling, characterized by the coefficient α_0, is illustrated by a MATLAB model in Chapter 2.2. An HSPICE simulation for different TSV pitches is also shown in Figure 2.12. As compared to Figure 2.11, the data shown in Figure 2.12 behaves in a similar manner, verifying the validity of the proposed MATLAB model.

Chapter 3

3.1 Summary

The application of swizzling to a 3-D TSV-based data bus is discussed in this thesis. Background knowledge about 3-D ICs, TSVs, TSV-based data buses, and swizzling is provided. An optimal swizzling pattern, minimizing the peak coupling noise, is proposed. The efficiency of swizzling for different TSV diameters, aspect ratios, and switching speeds of the signal along an aggressor line is demonstrated through HSPICE simulations. A MATLAB model is also provided to analyze the effects of TSV pitch on the efficiency of swizzling. The validity of the MATLAB model is verified through HSPICE simulations. Overall, swizzling is a *conditionally* efficient method for reducing peak coupling noise in a TSV-based 3-D data bus. The significant reduction in peak coupling noise suggests the potential of a TSV data bus with swizzling for future 3-D ICs.

3.2 Future research

As future research, developing a closed-form expression of the peak coupling noise in a TSV data bus may suggest more efficient swizzling patterns. If the noise on the adjacent lines can be controlled to switch in the opposite direction, namely, forcing the phase difference between the capacitive and inductive coupling noise to 180^o, the crosstalk noises can be significantly decreased. Closed-form expressions characterizing peak crosstalk noise in CMOS VLSI circuits have been proposed [66], [67]. These research ideas can also be applied to TSV data buses in 3-D ICs. The peak coupling noise is affected by the impedance of the bit line, which can be controlled by the swizzling patterns. This characteristic provides another hint to develop more efficient swizzling patterns.

Published research on swizzling patterns [15], [68] generally assumes an aggressor line or a post-processing algorithm for routing. However, a swizzling pattern cannot be changed after manufacture (unless it is made adaptive, which represents another research opportunity). Therefore, the ideal swizzling pattern should be uniform and signal independent. The patterns proposed in this thesis have a fixed number of swizzling events, which equals the width of a data bus minus two. This rigidity constrains the wide application of swizzling to 3-D ICs. For example, within an eight bit data bus through a three layer 3-D IC, the largest number of swizzling events is two instead of six. All of these drawbacks provide a direction for future research on TSV data buses in 3-D ICs.

A mixed structure composed of 2.5-D ICs [69] and 3-D ICs can be proposed to overcome these issues of swizzling patterns in 3-D ICs. For a 2.5-D IC, the horizontal portion of a data bus is handled by an interposer layer. The horizontal and vertical portions are connected by bumps. If the interposer is changeable, assuming each interposer has a particular swizzling pattern, the interposer layer can be switched to change the swizzling pattern. If the interposer is unchangeable, the layer can be composed of a special kind of material. When a signal arrives, the structure of this material can be changed and several channels for the electron motion can be produced.

Depending on different inputs, various channels are produced for signal propagation, which operate similar to a swizzled data bus.

Although swizzling of TSV data buses in 3-D ICs is not sufficiently mature, as circuits and materials evolve, TSV-based data buses will become more common. With the aid of swizzling, TSV data buses will be able to exhibit higher speed and integrity inter-layer communication within 3-D ICs.

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Appendix A

Decoupling in non-swizzled and swizzled TSV data buses

To decouple the data buses and determine the impedances, the assumption that each bit line of the data bus functions as both an aggressor and a victim is made.

A.1 Distribution of decoupled parallel TSV columns

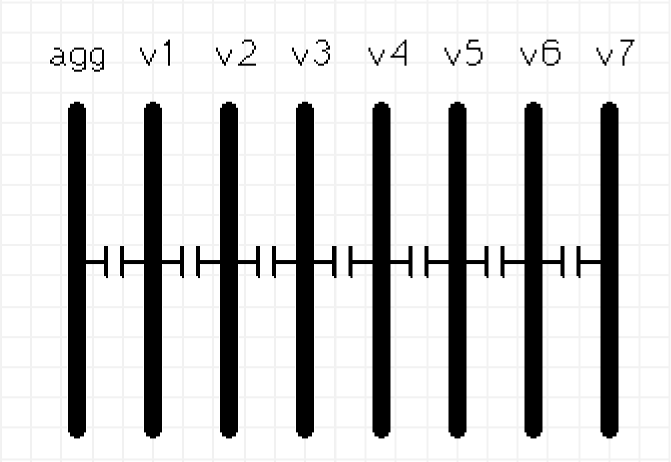

Figure A.1. Parallel TSV columns

According to the decoupling technique described in Chapter 1.4.3, after decoupling, the inductance L_i of each decoupled bit line is:

$$L_0 = L_{self} + L_{m1} + L_{m2} + L_{m3} + L_{m4} + L_{m5} + L_{m6} + L_{m7}, \tag{A.1.1}$$

$$L_1 = L_{self} - L_{m1} + L_{m1} + L_{m2} + L_{m3} + L_{m4} + L_{m5} + L_{m6}, \tag{A.1.2}$$

$$L_2 = L_{self} - L_{m2} - L_{m1} + L_{m1} + L_{m2} + L_{m3} + L_{m4} + L_{m5}, \tag{A.1.3}$$

$$L_3 = L_{self} - L_{m3} - L_{m2} - L_{m1} + L_{m1} + L_{m2} + L_{m3} + L_{m4}, \tag{A.1.4}$$

$$L_4 = L_{self} - L_{m4} - L_{m3} - L_{m2} - L_{m1} + L_{m1} + L_{m2} + L_{m3}, \tag{A.1.5}$$

$$L_5 = L_{self} - L_{m5} - L_{m4} - L_{m3} - L_{m2} - L_{m1} + L_{m1} + L_{m2}, \tag{A.1.6}$$

$$L_6 = L_{self} - L_{m6} - L_{m5} - L_{m4} - L_{m3} - L_{m2} - \boxed{L_{m1} + L_{m1},} \tag{A.1.7}$$

$$L_7 = L_{self} - L_{m7} - L_{m6} - L_{m5} - L_{m4} - L_{m3} - L_{m2} - L_{m1}. \tag{A.1.8}$$

Simplifying each expression,

$$L_0 = L_{self} + L_{m1} + L_{m2} + L_{m3} + L_{m4} + L_{m5} + L_{m6} + L_{m7}, \tag{A.1.9}$$

$$L_1 = L_{self} + L_{m2} + L_{m3} + L_{m4} + L_{m5} + L_{m6}, \tag{A.1.10}$$

$$L_2 = L_{self} + L_{m3} + L_{m4} + L_{m5}, \tag{A.1.11}$$

$$L_3 = L_{self} + L_{m4}, \tag{A.1.12}$$

$$L_4 = L_{self} - L_{m4}, \tag{A.1.13}$$

$$L_5 = L_{self} - L_{m5} - L_{m4} - L_{m3}, \tag{A.1.14}$$

$$L_6 = L_{self} - L_{m6} - L_{m5} - L_{m4} - L_{m3} - L_{m2}, \tag{A.1.15}$$

$$L_7 = L_{self} - L_{m7} - L_{m6} - L_{m5} - L_{m4} - L_{m3} - L_{m2} - L_{m1}. \tag{A.1.16}$$

The capacitance C_i of each decoupled bit line is

$$C_0 = C_{self}, \tag{A.1.17}$$

$$C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_7 = C_{self} + 2C_{coupling}. \tag{A.1.18}$$

The aggressor line is assumed to be the first bit line. L_{mi} is the mutual inductance when the distance between two TSV bit lines is i times the pitch.

A.2 Impedance distribution of decoupled TSV data buses

Based on A.1, the total capacitance and inductance of each signal path with no swizzling, swizzling patterns I and II, and the optimal pattern are determined. The inductance of the decoupled data paths is different while the capacitance is almost the same.

A.2.1 No swizzling pattern

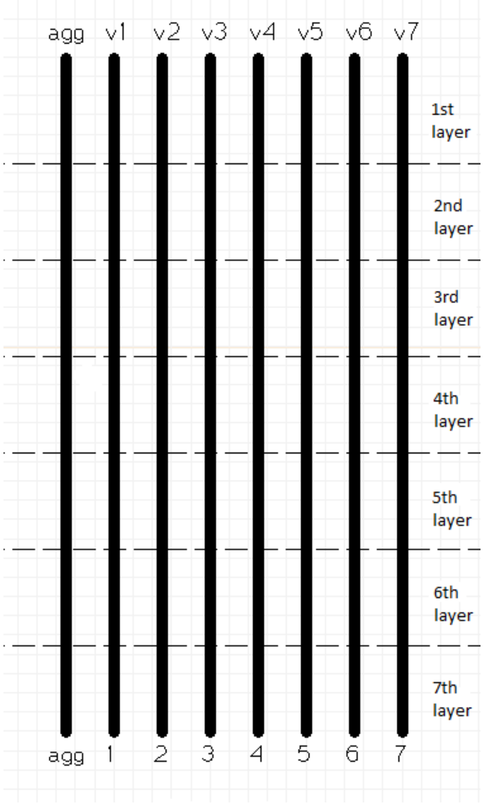

Figure A.2. No swizzling pattern.

$$L_{agg} = 7L_1, \tag{A.2.1}$$

$$L_{vic1} = 7L_1, \tag{A.2.2}$$

$$L_{vic2} = 7L_2, \tag{A.2.3}$$

$$L_{vic3} = 7L_3, \tag{A.2.4}$$

$$L_{vic4} = 7L_4, \tag{A.2.5}$$

$$L_{vic5} = 7L_5, \tag{A.2.6}$$

$$L_{vic6} = 7L_6, \tag{A.2.7}$$

$$L_{vic7} = 7L_7. \tag{A.2.8}$$

A.2.2 Swizzling pattern I

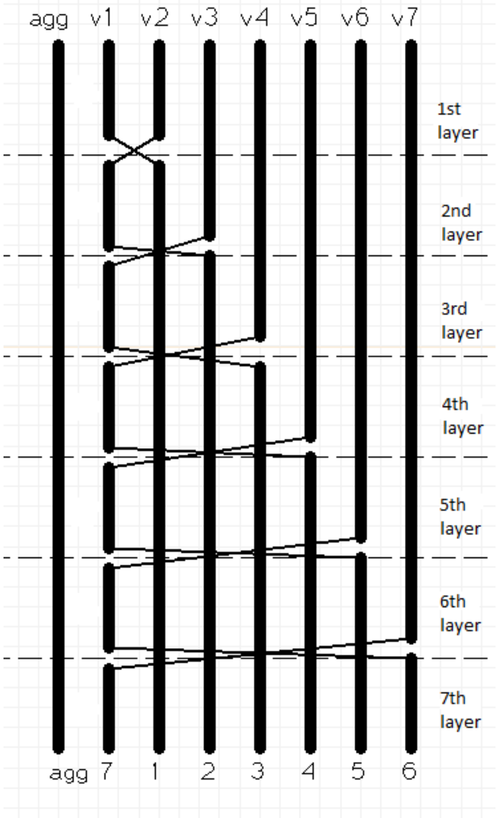

Figure A.3. Swizzling pattern I.

$$L_{agg} = 7L_1, \tag{A.2.9}$$

$$L_{vic1} = L_1 + 6L_2, \tag{A.2.10}$$

$$L_{vic2} = L_2 + L_1 + 5L_3, \tag{A.2.11}$$

$$L_{vic3} = 2L_3 + L_1 + 4L_4, \tag{A.2.12}$$

$$L_{vic4} = 3L_4 + L_1 + 3L_5, \tag{A.2.13}$$

$$L_{vic5} = 4L_5 + L_1 + 2L_6, \tag{A.2.14}$$

$$L_{vic6} = 5L_6 + L_1 + L_7, \tag{A.2.15}$$

$$L_{vic7} = 6L_7 + L_1. \tag{A.2.16}$$

A.2.2. Swizzling pattern II

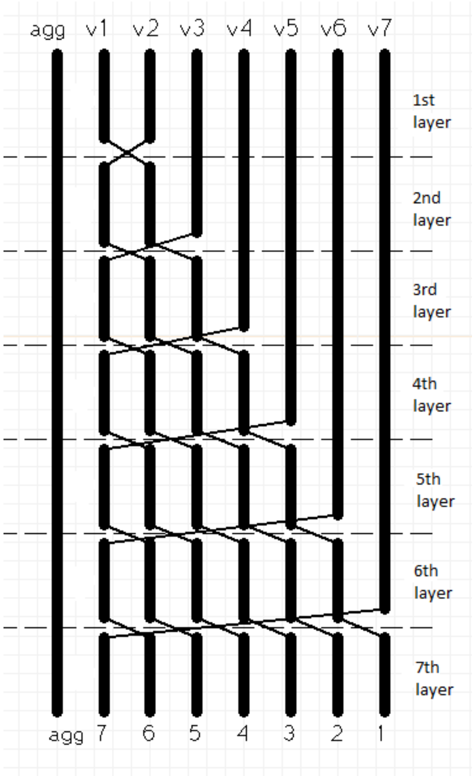

Figure A.4. Swizzling pattern II.

$$L_{agg} = 7L_1, \tag{A.2.17}$$

$$L_{vic1} = L_1 + L_2 + L_3 + L_4 + L_5 + L_6 + L_7, \tag{A.2.18}$$

$$L_{vic2} = L_2 + L_1 + L_2 + L_3 + L_4 + L_5 + L_6$$

$$= L_1 + 2L_2 + L_3 + L_4 + L_5 + L_6, \tag{A.2.19}$$

$$L_{vic3} = 2L_3 + L_1 + L_2 + L_3 + L_4 + L_5$$

$$= L_1 + L_2 + 3L_3 + L_4 + L_5, \tag{A.2.20}$$

$$L_{vic4} = 3L_4 + L_1 + L_2 + L_3 + L_4$$

$$= L_1 + L_2 + L_3 + 4L_4, \tag{A.2.21}$$

$$L_{vic5} = 4L_5 + L_1 + L_2 + L_3, \tag{A.2.22}$$

$$L_{vic6} = 5L_6 + L_1 + L_2, \tag{A.2.23}$$

$$L_{vic7} = 6L_7 + L_1. \tag{A.2.24}$$

A.2.3 Optimal swizzling pattern

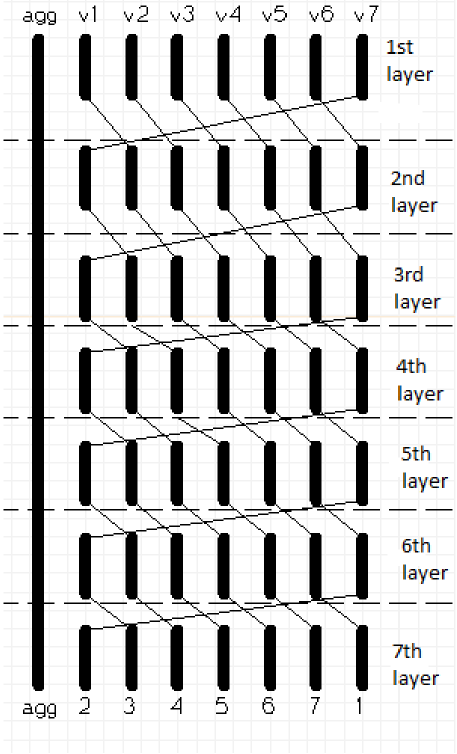

Figure A.5. Optimal swizzling pattern.

$$L_{agg} = 7L_1, \tag{A.2.25}$$

$$L_{vic1} = L_{vic2} = L_{vic3} = L_{vic4} = L_{vic5} = L_{vic6} = L_{vic7_1}$$

$$= L_1 + L_2 + L_3 + L_4 + L_5 + L_6 + L_7. \tag{A.2.26}$$

A.3 Discussion

The inductance of the four cases is listed in Table A.1. Based on the resistance, capacitance, and inductance of each signal path of a TSV data bus, the impedance is

$$Z = R + j\omega L + \frac{1}{j\omega C} \quad . \tag{A.3.1}$$

Although the impedance describes one individual path while the coupling noise is subject to the interrelated activity between two paths, the impedance of each individual path after decoupling is dependent on the coupling parameters. The impedance is therefore a reasonable criterion to evaluate the significance of coupling. Verified through HSPICE simulation, the peak noise generally appears on the bit line with the maximum impedance.

Table A.1. Inductance of each signal path in a decoupled TSV data bus

Inductance	No Swizzling	Pattern I	Pattern II	Optimal Pattern
Aggressor	$7(L_{self}+L_{m2}+L_{m3}+L_{m4}+L_{m5}+L_{m6})$	$7(L_{self}+L_{m2}+L_{m3}+L_{m4}+L_{m5}+L_{m6})$	$7(L_{self}+L_{m2}+L_{m3}+L_{m4}+L_{m5}+L_{m6})$	$7(L_{self}+L_{m2}+L_{m3}+L_{m4}+L_{m5}+L_{m6})$
Victim1	$7(L_{self}+L_{m2}+L_{m3}+L_{m4}+L_{m5}+L_{m6})$	$7L_{self}+L_{m2}+7L_{m3}+7L_{m4}+7L_{m5}+L_{m6}$	$7L_{self}-L_{m1}-L_{m2}-L_{m3}-L_{m4}-L_{m5}-5L_{m6}-L_{m7}$	$7L_{self}-L_{m7}-L_{m6}-L_{m5}-L_{m4}-L_{m3}-L_{m2}-L_{m1}$
Victim2	$7(L_{self}+L_{m3}+L_{m4}+L_{m5})$	$7L_{self}+L_{m2}+2L_{m3}+7L_{m4}+2L_{m5}+L_{m6}$	$7L_{self}+L_{m3}+L_{m4}+L_{m5}$	$7L_{self}-L_{m7}-L_{m6}-L_{m5}-L_{m4}-L_{m3}-L_{m2}-L_{m1}$
Victim3	$7(L_{self}+L_{m4})$	$7L_{self}+L_{m2}+L_{m3}-L_{m4}+L_{m5}+L_{m6}$	$7L_{self}+L_{m2}+L_{m3}+3L_{m4}+L_{m5}+L_{m6}$	$7L_{self}-L_{m7}-L_{m6}-L_{m5}-L_{m4}-L_{m3}-L_{m2}-L_{m1}$
Victim4	$7(L_{self}-L_{m4})$	$7L_{self}+L_{m2}-2L_{m3}-5L_{m4}-2L_{m5}+L_{m6}$	$7L_{self}+L_{m2}+2L_{m3}-L_{m4}+2L_{m5}+L_{m6}$	$7L_{self}-L_{m7}-L_{m6}-L_{m5}-L_{m4}-L_{m3}-L_{m2}-L_{m1}$
Victim5	$7(L_{self}-L_{m5}-L_{m4}-L_{m3})$	$7L_{self}-L_{m2}-5L_{m3}-5L_{m4}-5L_{m5}-L_{m6}$	$7L_{self}+L_{m2}-2L_{m3}-L_{m4}-2L_{m5}+L_{m6}$	$7L_{self}-L_{m7}-L_{m6}-L_{m5}-L_{m4}-L_{m3}-L_{m2}-L_{m1}$
Victim6	$7(L_{self}-L_{m6}-L_{m5}-L_{m4}-L_{m3}-L_{m2})$	$7L_{self}-L_{m1}-5L_{m2}-5L_{m3}-5L_{m4}-5L_{m5}-5L_{m6}-L_{m7}$	$7L_{self}-4L_{m2}-3L_{m3}-3L_{m4}-3L_{m5}-4L_{m6}$	$7L_{self}-L_{m7}-L_{m6}-L_{m5}-L_{m4}-L_{m3}-L_{m2}-L_{m1}$
Victim7	$7(L_{self}-L_{m7}-L_{m6}-L_{m5}-L_{m4}-L_{m3}-L_{m2}-L_{m1})$	$7L_{self}-6L_{m1}-5L_{m2}-5L_{m3}-5L_{m4}-5L_{m5}-5L_{m6}-6L_{m7}$	$7L_{self}-6L_{m1}-5L_{m2}-5L_{m3}-5L_{m4}-5L_{m5}-5L_{m6}-6L_{m7}$	$7L_{self}-L_{m7}-L_{m6}-L_{m5}-L_{m4}-L_{m3}-L_{m2}-L_{m1}$