Low Power Quasi-Resonant Interconnects

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A primary challenge in high performance, high complexity integrated circuits is the on-chip interconnect [1]. Transmitting clock, data, and communications signals over large die areas requires long interconnections among the various circuit modules. Consequently, as technology scales, the interconnect cross section decreases while operating frequencies have increased. The impact of these trends on high performance systems is significant. Long interconnects with smaller cross sections exhibit increased capacitance and resistance, resulting in greater power consumption, latency, and signal attenuation. Furthermore, wire inductance can no longer be ignored, due to high signal frequencies and long wire lengths [2].

To combat these phenomena, traditional repeater insertion methods have been implemented. Low power techniques in the form of low swing signaling and optoelectronic links [3] have also been considered. An alternative approach exploiting wire inductance at high frequencies is introduced in [4-5].

A low power quasi-resonant design methodology is proposed in this paper. The interconnect capacitance resonates with the inserted on-chip inductance. This approach lowers the power consumption, since the energy resonates between the electric and magnetic fields rather than dissipated as heat.

The design methodology is based on a shielded interconnect with a capacitive load, driven by a buffer such that the fundamental harmonic of the input bit stream is transferred to the output. The output signal at the far-end exhibits a sinusoidal behavior. An inverter is placed at the far-end of the line to convert a sinusoidal waveform into an inverted square bit stream. An on-chip spiral inductor is used to resonate the data signal around the harmonic frequency, eliminating the need for repeaters and complex circuitry at the transmitter and receiver ends of the line.

The return to zero (RZ) amplitude shift keying modulation scheme is chosen to support a single targeted transmission frequency of the input data. In this scheme, the data is transferred at $1/t_p$ bits per second.



Figure 2. Resonant transmission line: (a) Layout geometry, (b) Equivalent *RLC* model

The layout geometry as well as a model of the resonant interconnect network are depicted in Figure 2. The interconnect is represented by a distributed *RLC* transmission line, where *l* is the interconnect length, and *R*, *L*, and *C* are the resistance, inductance, and capacitance per unit length, respectively. The driver is linearized as a

voltage source V_d serially connected with a driver resistance R_d . The load of the interconnect is modeled as a capacitor C_l . Note that the on-chip inductor is inserted at a distance l_d from the driver to resonate the data signal at a specific transmission frequency.

A comparison between the proposed methodology and other approaches in the literature is listed in Table 1. Interestingly, a maximum reduction in power consumption of 98.5% and a 60% reduction in delay is demonstrated for quasi-resonant interconnects as compared to optoelectronic links [3]. The power consumption overhead in [3] is caused by the edge emitting laser modulator at the transmitting edge and the photodiode and signal level restorer at the receiving end of the optical link. This example may suggest that using novel signaling schemes incorporating electrical interconnects can outperform optoelectronic solutions. Lower power is achieved despite the optical link transmitting a slower signal (3 Gbps) as compared to the resonant link (5 Gbps). As listed in Table 1, the proposed quasi-resonant interconnect methodology outperforms other approaches described in the literature in both power and latency.

Table 1. Performance comparison of quasi-resonant method with different approaches

	Technology	Speed [Gbps]	Length [mm]	Power [mW]	Delay [ps]
Quasi-resonant	180 nm	5	3	0.75	76
Pulsed current [4]	180 nm	8	3	27.12	280
Improvement				97.2%	72.8%
Quasi-resonant	180 nm	5	17	3.7	231
Signal modula- tion [5]	180 nm	1	20	16	300
Improvement				76.9%	23.0%
Quasi-resonant	180 nm	5	5	1.17	104
Optics (edge emitting) [3]	250 nm	3	5	78	260
Improvement				98.5%	60.0%
Quasi-resonant	180 nm	5	5	1.17	104
Optics (VCSEL) [3]	250 nm	3	5	66	300
Improvement				98.2%	65.3%

REFERENCES

- [1] The International Technology Roadmap for Semiconductors (ITRS), 2006
- [2] Y. I. Ismail and E. G. Friedman, "Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits," *IEEE Transactions* on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 2, pp. 195-206, April 2000
- [3] E. D. Kyriakis-Bitzaros, N. Haralabidis, M. Lagadas, A. Georgakilas, Y. Moisiadis, and G. Halkias, "Realistic End-to-End Simulation of the Optoelectronic Links and Comparison with the Electrical Interconnections for System-on-Chip Applications," *IEEE Journal of Lightwave Technology*, Vol. 19, No. 10, pp. 1532-1542, October 2001
- [4] R. T. Chang, N. Talwalker, C. P. Yue, and S. S. Wong, "Near Speed-of-Light Signaling Over On-Chip Electrical Interconnects," *IEEE Journal* of Solid-State Circuits, Vol. 38. No. 5, pp. 834-838, May 2003
- [5] A. P. Jose, G. Patounakis, and K. L. Shepard, "Near Speed-of-Light On-Chip Interconnects Using Pulsed Current-Mode Signaling," *Proceed*ings of the IEEE Symposium on VLSI Circuits, pp. 108-111, June 2005