On-die Decoupling Capacitance: Frequency Domain Analysis of Activity Radius

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Abstract-On-die capacitances interact with the inductance and resistance of the power distribution network to supply electrical charge. A distributed model is generally required to analyze and design a power distribution network to maintain acceptable levels of supply voltage noise. An approximation method is proposed in this paper for modeling the power distribution system in the frequency domain, defining an effective decoupling capacitance and an effective decoupling radius around each switching element, both of which are frequency dependent. At high frequencies, the supply of decoupling charge is highly localized, and the effective decoupling capacitance is determined primarily by the power grid inductance. Design considerations and guidelines are presented for determining the appropriate density of on-die decoupling capacitances and required power grid parameters, depending upon the density and the frequency characteristics of the switching activity of the circuit.

I. INTRODUCTION

Current consumption is constantly rising together with clock frequencies in modern VLSI circuits. The power distribution network is required to have a low impedance resonance-free profile over a wide frequency range. This target impedance is achieved by decoupling capacitances at the board, package, and die levels. At high operating frequencies, the on-die elements must be treated as a distributed system. The on-die power grid, presented schematically in Figure 1, exhibits both a resistive and inductive nature [1].



Fig. 1. On-die power grid schematic center view

The power grid is typically uniform and symmetric in the X-Y directions on a die surface. On-die decoupling capacitances supply locally stored charge for fast current transients. The capacitances are generally of two types: symbiotic and intentional. Symbiotic decoupling capacitance is provided by existing devices and interconnects within idle logic circuitry [2-4]. Intentional Mikhail Popovich, Eby G. Friedman

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capacitance is provided by specially designed circuits whose primary role is decoupling. The sum of both types is the on-die decoupling capacitance. Unlike board and package level decoupling capacitors, on-die capacitance is distributed all over the circuit. In this paper, the on-chip decoupling capacitors are assumed to be uniformly distributed with a density of C_{die} per unit area. This assumption, however, does not imply that each circuit or functional block uses only the local C_{die} portion, since all local C_{die} elements are connected into a unified pool by the power grid (see Figure 2).



Fig. 2. Simplified effective capacitance model: (left) - power distribution network structure and distributed C_{die} around a single switching circuit modeled by a current source; (right) - an approximate model of a frequency-dependent effective capacitance

Sharing of the C_{die} is limited because of the localized nature of the decoupling capacitance. The power grid provides the connections, but adds a local impedance in series with remote portions of C_{die} . These additional impedances reduce the effectiveness of the remote C_{die} , such that the charge supplied to the switching circuit from a distance gradually becomes negligible. Hence, it is important to define metrics of effectiveness for the decoupling capacitance.

A properly designed network can be characterized by a flat impedance profile over a wide frequency range. In this paper, it is assumed that a bound for the switching current spectrum $I(\omega)$ can be estimated, and the local power delivery network impedance $Z(\omega)$ can be designed such that at each frequency, the power supply noise is

$$V_n(\omega) = I(\omega) \cdot Z(\omega) . \tag{1}$$

The on-die power network components are dependent upon the high frequency behavior of the impedance, typically well above hundreds of MHz [4]. The complex power distribution network can be approximated by a lumped effective capacitance $C_{eff}(\omega)$, comprised of the C_{die} elements contained within an effective radius r_{eff} around the switching circuit, as illustrated in Figure 2. In this case, the power distribution network impedance is

$$Z(\omega) = \frac{1}{i\omega \cdot C_{eff}(\omega)},$$
(2)

and the high frequency on-die voltage noise can be found by integrating over the corresponding frequency range,

$$V_{n_die} = \int_{\omega_die} I(\omega) \cdot Z(\omega) d\omega = \int_{\omega_die} I(\omega) \cdot \frac{1}{i\omega \cdot C_{eff}(\omega)} d\omega .$$
(3)

A similar approach was used in [8] to evaluate the effectiveness of a lumped decoupling capacitor on a printed circuit board as a function of the distance of the capacitor from the switching circuits. The primary difference between these two problems is that in the off-die (board-level) case, the decoupling capacitor is lumped and the current loads are distributed, while in the on-die case the decoupling capacitance is also distributed. Also, off-die inductance is typically high while on-die inductance is low.

Accurate modeling and simulation of the power grid is a complicated computational task. An approach for estimating the effective radius r_{eff} and effective decoupling capacitance C_{eff} , is presented in this paper. This approach is based on the assumption that the power grid is a dense structure represented by uniform parameters per unit area.

The rest of this paper is organized as follows: an analysis of the power grid is presented in section II, focusing on the effective radius r_{eff} and the effective decoupling capacitance C_{eff} . The results are validated by circuit simulation of an example power grid in section III. Some conclusions are offered in section IV.

II. ON-DIE POWER NETWORK ANALYSIS

A. Power Grid representation and analysis

An on-chip power grid consists of metal interconnect within different layers, connected by vertical vias as shown in Figure 1. Typically, any two adjacent metal layers are perpendicularly oriented, in both *VCC* (Power) and *VSS* (Ground). A grid composed of only two metal layers is discussed here. An electrical schematic representing the power grid, particularly the resistive and inductive nature, is presented in Figure 3 (left).





All of the circuit elements, including the current loads (the switching circuits) and the decoupling capacitances, are connected between the power and ground nets. A simplified representation of a single grid segment is illustrated in Figure 3 (left). The characteristic size of such a segment is determined by an interconnect section between two neighboring vias. The power grid structure includes numerous vias; hence, the number of basic power grid cells can be extremely large, leading to extremely high complexity in the electrical representation of the network.

A dense power grid can be represented as a continuous structure. The Power (VCC) and Ground (VSS) nets can be represented by planes with a sheet resistance and inductance equivalent to those of the original grid. The same approach can be applied to the decoupling capacitors, which can be modeled as a continuous capacitive layer. Thus, the entire structure of the power network can be represented as a pair of parallel planes (the network Power/Ground grids) and the space between the grids represents the distributed impedance of the decoupling capacitors, as shown in Figure 3 (right). In contrast to the original network structure, this continuous structure can be characterized by a current density at each point rather than by numerous discrete branch currents. Since the model is linear, the system can be solved in the frequency domain. At each frequency, the planes can be represented by an effective sheet resistance in units of $[\Omega/\Box]$,

$$S_{grid} = R_{grid} + i\omega \cdot L_{grid} , \qquad (4)$$

where R_{grid} and L_{grid} are the characteristic resistance and inductance, respectively, of a power and ground grid segment.

Similarly, the impedance of the decoupling capacitance is represented by a layer of material with an equivalent specific resistivity ρ_{die} and length *L*. Assuming *L* =1 (see Figure 4),

$$\rho_{die} = R_{die} + \frac{1}{i\omega \cdot C_{die}}, \qquad (5)$$

where R_{die} and C_{die} are the effective series resistance (ESR) and the density of the uniformly distributed on-die decoupling capacitance. As the decoupling capacitance is characterized by a density per unit area, the units of ρ_{die} are $[\Omega^*\mu m]$.

The effective decoupling radius is significantly smaller than a typical modern VLSI die size [5]. The system can therefore be treated as infinite, with no boundary effects. Under these conditions, any local effect caused by a single internal excitation only depends on distance from the load to the capacitance. Hence, a cylindrical structure rather than rectangular is assumed, as shown in Figure 4. Radial symmetry is also assumed based on uniformity of all of the parameters in the system.



Fig. 4. Equivalent electrical representation of a uniform power grid with uniform decoupling capacitance

The currents being evaluated are characterized at each point of the system, with densities $j_{grid}(r)$ and $j_{die}(r)$ in the power grid and on-die decoupling capacitance, respectively. The conducting layer can be analyzed as a set of narrow rings. Current through a ring with radius r is composed of current $i_{grid}(r)$ in the horizontal direction and

 $i_{die}(r)$ in the vertical direction (see Figure 4). Current which passes horizontally through the ring with radius *r* is

$$i_{grid}(r) = 2\pi \cdot r \cdot j_{grid}(r) .$$
(6)

From the principle of current conservation, the change of current in each ring is due to the current which flows down through the die to the bottom layer, with a density $j_{die}(r)$. Thus,

$$\frac{di_{grid}(r)}{dr} = -2\pi \cdot r \cdot j_{die}(r) .$$
(7)

Kirchhoff's voltage law for two neighboring rings with radii r_1 and r_2 , respectively, leads to

 $j_{die}(r_1) \cdot \rho_{die} = j_{grid}(r_1) \cdot \rho_{S_grid} \cdot (r_2 - r_1) + j_{die}(r_2) \cdot \rho_{die}$, (8) where ρ_{S_grid} represents the impedance of both *VCC* and *VSS* layers.

Transforming (8) while $(r_2 - r_1)$ approaches zero, using (7) and differentiating (6),

$$j''_{die}(r) + \frac{j'_{die}(r)}{r} = a^2 j_{die}(r)$$
(9)

where $a^2 = \frac{\rho_S}{\rho_{die}}$. The units of the parameter *a* are

 $[\mu m^{-1}]$. Therefore, the expression $(a \cdot r)$ is dimensionless. As $\rho_{S_{grid}}$ and ρ_{die} are frequency dependent (see (4) and (5)), the value of *a* is also frequency dependent.

The character of the solution of Eq. (9) differs accordingly to whether a^2 is real, imaginary or complex. At relatively low frequencies, such that the power grid impedance is predominantly resistive (e.g. below 1 Ghz [6]), $a^2 = \frac{\rho_S}{-grid} / \rho_{die} = i\omega \cdot C_{die} \cdot R_{grid}$, *a* is an imaginary number. Consequently this expression becomes Kelvin's

equation of zero order with a solution of the form

$$die(r) = j_0 \bullet [Ker_0(a \bullet r) + i \bullet Kei_0(a \bullet r)], \qquad (10)$$

where Ker_0 and Kei_0 are Bessel Kelvin functions and j_0 is determined by the source term. The absolute value of the current density is plotted in Figure 5, exhibiting expected localization.



Fig. 5. Current magnitude as a function of radius for a resistive grid At high frequencies where the power grid is dominated by inductance [6], a^2 is a negative real value $a^2 = \frac{\rho_{S-grid}}{\rho_{die}} = -\omega^2 \cdot C_{die} \cdot L_{grid}$. Expression (9) becomes Bessel equation of zero order. Considering

becomes Bessel equation of Zero order. Considering boundary conditions, the solution is

$$j_{die}(r) = j_0 \cdot H_0^{(2)}(a \cdot r) , \qquad (11)$$

where $H_0^{(2)}$ is the zero order Hankel function of the second kind. This solution is plotted in Figure 6, also exhibiting localization at small radii. This localization allows defining an effective decoupling radius.



Fig. 6. Current magnitude as a function of radius for an inductive grid

B. Definition of effective decoupling radius r_{eff}

The average power at radius r is proportional to

$$P(r) \propto 2\pi \cdot r \cdot |j_{die}(r)|^2 . \tag{12}$$

For a resistive grid, the energy flux corresponding to (10) is plotted in Figure 7 versus $a \cdot r$.

2π•a•r•|Ker(a•r)+i•Kei(a•r)|² - normalized



Fig. 7. Average power as a function of radius in a resistive grid The effective radius is defined in this case such that just 10% of the peak energy flux is contained out the circle of radius r_{eff} . It corresponds to $a \cdot r = 2.1$. Hence, substituting (4) and (5) into (12) and neglecting R_{die} [2, 3],

$$f_{eff_RES} = 2.1 \cdot \frac{1}{\sqrt{\omega \cdot C_{die} \cdot R_{grid}}}$$
(13)

The effective radius $r_{eff.RES}$ diminishes with higher power grid resistance. Intuitively, the higher grid impedance effectively prevents current from being widely distributed. Also, a higher decoupling capacitance density C_{die} leads to a smaller effective radius since a higher density of decoupling capacitances provides more effective shunting and thus a smaller dispersion radius.

A similar calculation for the case of dominantly inductive grid is presented in Figure 8.



Fig. 8. Average power as a function of radius in an inductive grid In this case

$$r_{eff_IND} = 0.75 \cdot \frac{1}{\sqrt{\omega \cdot C_{die} \cdot \omega \cdot L_{grid}}} = \frac{0.75}{\omega} \cdot \frac{1}{\sqrt{C_{die} \cdot L_{grid}}}$$
(14)

In both cases, the effective radius r_{eff} becomes smaller with frequency.

C. Effective Decoupling Capacitance C_{eff}

Once the effective radius r_{eff} and current density $j_{die}(r)$ are known for the continuous problem, these parameters can be used to explore the original power grid problem. The effective radius, power grid characteristics R_{grid} and L_{grid} , decoupling capacitance density C_{die} and operating frequency ω are all interrelated.

An approximate estimate of the effective decoupling capacitance $C_{eff RES}$ for low frequencies is

$$C_{eff_RES} = \pi \cdot r_{eff_RES}^2 \cdot C_{die} = \pi \left(21 \cdot \frac{1}{\sqrt{\omega} \cdot C_{die} \cdot R_{grid}} \right)^2 \cdot C_{die} \propto \frac{1}{\omega \cdot R_{grid}}.$$
 (15)

At high frequencies, $R_{grid} \ll \omega \cdot L_{grid}$ and

$$C_{eff_IND} = \pi \cdot r_{eff_IND}^2 \cdot C_{die} = \pi \left(\frac{0.75}{\omega} \cdot \frac{1}{\sqrt{C_{die} \cdot L_{grid}}} \right)^2 \cdot C_{die} \propto \frac{1}{\omega^2 \cdot L_{grid}},$$
(16)

exhibiting an inverse dependence on ω^2 . Physically, the inverse dependence of the effective decoupling C_{eff} on frequency becomes greater when inductive effects dominate resistive effects. Another observation from (15) and (16) is that C_{eff} does not depend on C_{die} . Intuitively, the larger C_{die} should increase C_{eff} but the larger C_{eff} leads to a lower impedance of the decoupling capacitance and thus to a lower voltage drop, and less charge is released into the power grid from the decoupling capacitance. The effective radius is infinite without any decoupling capacitance.

III. NUMERICAL SIMULATION OF A POWER GRID

In order to validate the results of this analysis, approach, an example power grid has been numerically simulated. An RL model is created by extraction of two metal layers 500µm by 500µm structure of 0.6 µm width wires, forming an interleaved power grid with 3 µm spacing, in an industrial 65 nm process. The characteristic grid impedance parameters are $R_{grid}=10\Omega$ and $L_{grid}=0.55pH$. The decoupling capacitance elements are distributed uniformly within the grid. Circuit simulation is performed in the frequency domain. The resultant current density distribution as a function of radius for several frequencies is shown in Figure 9. Clearly, localization is more pronounced at high frequencies.



ig 9. Current density as a function of fadius – simulation result

IV. DISCUSSION AND CONCLUSIONS

Numerous current loads exist in every integrated circuit. Each load circuit is placed in a specific area and provides some local decoupling capacitance [7]. A set of uniformly distributed current loads is presented in the example characterized in Figure 9. Each current load is placed in the middle of a virtual cell, defined as the neighborhood around the switching circuit block. In the worst case, all of these current loads act simultaneously with no sharing. Two design requirements from the power delivery network are necessary. First, the effective radius r_{eff} of the decoupling capacitance has to be smaller than or equal to the dimension of the "activity cell" (see Figure 10), to avoid interference among the cells. Second, the effective decoupling capacitance inside each cell has to be sufficiently large in order to satisfy the voltage noise design target within the appropriate range of frequencies.

Knowledge of the current load density in the circuit, depending on the circuit types and logic activity, determines the activity cell size and hence the required r_{eff} . Targets for the power grid parameters, R_{grid} and L_{grid} , and the decoupling capacitance C_{die} can be set according to (13) and (14), in order to satisfy the first requirement. Note that the second requirement cannot be satisfied by uniformly adding extra decoupling capacitance C_{die} , since this method would only reduce the effective decoupling radius. More effective decoupling can be provided only by lowering the power grid impedances, according to (15) and (16).



Fig 10. Conceptual partitioning of the area into activity cells

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REFERENCES

- A. Mezhiba and E. G. Friedman, "Power Distribution Networks in High Speed Integrated Circuits," Kluwer Academic Publishers, 2004.
- [2] W. Dally and J. Poulton, "Digital Systems Engineering," Cambridge University Press, 1998, pp.160-161, 244-245.
- [3] M. Sotman, M. Popovich, A. Kolodny, and E. Friedman, "Leveraging Symbiotic On-Die Decoupling Capacitance," Proceedings of the IEEE conference on Electrical Performance of Electronic Packaging, October 2005.
- [4] A. Waizman and C.-Y. Chung, "Resonant Free Power Network Design Using Extended Adaptive Voltage Positioning (EAVP) Methodology," *IEEE Transactions on Advanced Packaging*, Volume 24, Issue 3, pp. 236-244, Aug. 2001.
- [5] E. Chiprout, "Fast Flip-Chip Power Grid Analysis via Locality and Grid Shells", *IEEE Transactions on Computer Aided Design*, pp. 485 – 488, Nov. 2004.
- [6] L. Zlydina and Y. Yagil, "3D power grid modeling," Proceedings of the IEEE Conference on Electronics, Circuits and Systems, 13-15, pp. 129 – 132, Dec. 2004.
- [7] Shiyou Zhao, K. Roy and Cheng-Kok Koh, "Decoupling capacitance allocation and its application to power-supply noiseaware floorplanning," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Volume 21, Issue 1, pp. 81 – 92, Jan. 2002.
- [8] H. Chen, J. Fang, and W. Shi, "Effective decoupling radius of decoupling capacitor," *Proceedings of the IEEE Conference on Electrical Performance of Electronic Packaging*, 29-31, pp. 277– 280, Oct 2001.