Superconductive Logic Using \(2\phi\)-Josephson Junctions with Half Flux Quantum Pulses

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Abstract—Superconductive logic based on Josephson junctions (JJ) is a promising technology for energy efficient supercomputers and cloud computing. This technology can deliver significant improvements in performance and energy efficiency as compared to CMOS. Superconductive circuits, however, suffer from low density integration as compared to CMOS, primarily due to the limited scalability of the inductors. To improve the scalability of superconductive logic, a logic family based on a novel JJ technology, \(2\phi\)-JJ, has been proposed that eliminates the inductors. In this paper, three circuits are presented which exploit this scalable inductor-less technology. This novel \(2\phi\)-JJ technology represents the data as half flux quantum (HFQ) pulses, which improves the energy efficiency and speed as compared to standard superconductive logic such as rapid single flux quantum (RSFQ). Unlike RSFQ, the proposed circuits dynamically switch upon receiving an HFQ pulse, saving energy. These \(2\phi\)-JJ logic circuits operate 2.25X faster and require 2.6X less energy as compared to RSFQ.

I. INTRODUCTION

Demand for energy efficient computation is growing, particularly for exascale supercomputers and cloud computing. A potential technology to achieve energy efficient, high performance computing is superconductive technology [1]. Rapid single flux quantum (RSFQ) [2], energy efficient RSFQ (ERSFQ) [3], and energy efficient single flux quantum (eSFQ) [4] are examples of energy efficient, high performance superconductive logic families. RSFQ circuits have been experimentally demonstrated to operate at frequencies up to 770 GHz [5] with die-to-die communication of more than 100 Gbit/s [6], [7]. The information in RSFQ circuits is represented as a voltage pulse with a quantized area equal to a single flux quantum (SFQ), \(\Phi_0 = \frac{\hbar}{2e}\). A logic 1 is characterized by the existence of an SFQ pulse while logic 0 is the absence of a pulse. The duration of an SFQ pulse can be as fast as 2 ps with a voltage magnitude of 1 mV, as illustrated in Fig. 1.

RSFQ circuits are primarily composed of Josephson junctions (JJs) and inductors. A significant drawback of RSFQ circuits is limited improvement in density due to the inability to scale inductors in modern superconductive fabrication technologies [8]. To improve density, superconductive circuits without inductors have been proposed [8]. These inductor-less circuits use a novel JJ called \(2\phi\)-JJ. Although the \(2\phi\)-JJ passes half flux quantum (HFQ) pulses, SFQ pulses are used at the input and output of the logic gate.

\(2\phi\)-JJ circuits produce, transmit, and represent data by HFQ pulses. Combining \(2\phi\)-JJs with standard JJs allows the proposed circuit technology to be scalable since inductors are not used. Several logic circuits, a Josephson transmission line (JTL), an inverter, and an OR gate, are proposed. Energy efficiency improvements of 2.6X and speed improvements of 2.25X as compared to RSFQ logic are achieved.

II. BEHAVIOR OF JOSEPHSON JUNCTION

The dynamic behavior of standard JJs and \(2\phi\)-JJs is explained, respectively, in Sections II-A and II-B.

A. Standard Josephson Junctions

A JJ is a multilayer device composed of a superconductive layer (S), an insulating layer (I), and a second superconductive layer (S). The JJ is described by the following expressions,

\[
I = I_c \sin (\phi), \quad (1)
\]

\[
\frac{d\phi}{dt} = \frac{2e}{\hbar} V, \quad (2)
\]

where \(I\) is the current in the JJ, \(I_c\) is the critical current of the JJ, \(\phi\) is the phase difference between the superconductive layers, \(e\) is the electron charge, \(\hbar\) is the Planck constant divided by \(2\pi\), and \(V\) is the voltage across the device.

From (1) and (2), the energy-phase relationship (EPR) of a junction is

\[
E_J = E_{J0}(1 - \cos (\phi)), \quad (3)
\]

\[
E_{J0} = \frac{\hbar I_c}{2e}. \quad (4)
\]

The minimum energy of the junction occurs at a \(2\pi n\) phase difference (0, \(2\pi, 4\pi \ldots\)), where \(n\) is an integer, as depicted in Fig. 2a.

The JJ can be represented by a resistively and capacitively shunted junction (RCSJ) model [9], as illustrated in Fig. 3. Based on the RCSJ model, (1), (2), and Kirchoff’s current law, the current of a JJ is

\[
I = I_c \sin \phi + \frac{1}{R} \frac{h \phi}{2e} \frac{d\phi}{dt} + C \frac{h}{2e} \frac{d^2\phi}{dt^2}. \quad (5)
\]
Applying a current greater than the critical current produces an SFQ voltage pulse, switching the phase of the junction by $2\pi$.

### B. $2\phi$-Josephson Junction

A JJ topology composed of a ferromagnetic (F) layer with a one spin active interface rather than an insulating layer exhibits a current-phase relationship (CPR) with a dominant second harmonic [10]–[14]. Robust junctions with a purely second harmonic [12], [15] have been experimentally demonstrated. Junctions with a second harmonic exhibit a CPR of

$$I = I_{c_1} \sin(\phi) + I_{c_2} \sin(2\phi),$$  

and an EPR of

$$E = I_{c_1}(1 - \cos(\phi)) + \frac{I_{c_2}}{2}(1 - \cos(2\phi)),$$  

where $E$ is normalized by the Josephson energy $E_{J_0}$, and $I_{c_1}$ and $I_{c_2}$ are the amplitude of each harmonic.

Junctions with a purely second harmonic are called $2\phi$-JJs. Unlike standard JJs, these junctions exhibit a minimum energy at a $\pi n$ phase difference, as illustrated in Fig. 2b. $2\phi$-JJs can be modeled using the same RCSJ model with a supercurrent, as described in (6). Based on the RCSJ model and solving (5) for a $2\phi$-JJ, the $2\phi$-JJ switches when a $\pi$ phase difference occurs, producing an HFQ voltage pulse. The HFQ pulse is half the area of an SFQ, and is produced when a junction switches by $\pi$ rather than $2\pi$. Unlike RSFQ, information in the proposed logic circuits is transmitted and stored as an HFQ pulse, which is more energy efficient than an SFQ pulse. The energy required for a standard JJ to switch by $2\pi$ is $E \approx \Phi_0 I_c$, while switching a $2\phi$-JJ by $\pi$ requires half of this energy.

### III. LOGIC CIRCUITS BASED ON $2\phi$-JJS

In this section, three logic circuits based on $2\phi$-JJs and standard JJs are proposed. The primary constraint in these circuits is that the phase within each superconductive loop must sum to $2\pi n \ (\ldots - 2\pi, 0, 2\pi \ldots)$, a fundamental requirement in superconductive loops. If the phase of the junctions does not add to $2\pi n$, a circulating current is produced to add or subtract the phase of the junctions until a phase of $2\pi n$ is achieved.

RSFQ logic gates are DC powered, individually clocked, and all of the junctions require a bias current below the critical current $I_c$. The characteristics of the proposed $2\phi$-JJ logic gates are similar to RSFQ gates. The proposed circuits contain $2\phi$-JJs based on $\pi$ phase switches. Standard JJs behave as an impedance and do not switch. This trait adds design complexity but enhances the energy efficiency and replaces the inductors. The following subsections introduce the three proposed circuits and operating principles along with simulations illustrating the circuit functionality.

#### A. Josephson Transmission Line (JTL)

The function of a JTL is as a local interconnect to connect nearby logic gates. The output of a logic gate is connected to the input of another logic gate by one or more JTLs [16]. In RSFQ circuits, a JTL stage is composed of two JJs connected by an inductor. In this proposed JTL circuit, two $2\phi$-JJs are connected by a standard JJ rather than by an inductor. The proposed circuit is illustrated in Fig. 4.

The circuit functions as follows. An HFQ pulse is received at the input; accordingly, a current pulse enters the circuit. Most of the current passes through the initial $2\phi$-JJ, $JJ_1$, since the first standard JJ is in a high impedance state. The phase of $JJ_1$ switches by $\pi$, propagating a current pulse through the standard JJ and switching the second $2\phi$-JJ, $JJ_2$. Each $2\phi$-JJ produces a current pulse which switches the following $2\phi$-JJ. After the pulse is transferred from the input to the output, the phase of each $2\phi$-JJ switches by $\pi$, as illustrated in Fig. 5. The inputs in Fig. 5 are modeled as an HFQ pulse; a triangular voltage pulse with an area of $\frac{\Phi_0}{2}$. The switching behavior of the $JJ_1$ switch is therefore different from the following $JJ$s.
Fig. 5: JTL circuit behavior, (a) voltage pulse, and (b) phase switch.

Fig. 6: Proposed inverter, (a) voltage, and (b) phase.

Fig. 7: Proposed inverter, (a) voltage, and (b) phase.

**B. Inverter**

The proposed inverter is a superconductive loop composed of two $2\phi$-JJs and two standard JJs. The additional $2\phi$-JJ, below the superconductive loop, is an output JJ, which produces and sends an HFQ pulse to the next logic gate. A schematic of the proposed inverter is shown in Fig. 6.

Once an HFQ pulse arrives at the input, most of the current proceeds through $JJ_{in}$ since the two serially connected JJs impose a high impedance on the current, switching $JJ_{in}$ by $\pi$. Two serial JJs are used because one standard JJ in the loop will not hold the HFQ pulse. A large circulating current would have been produced and switched $JJ_{clk}$ to acquire a phase of $2\pi$. However, with two serial JJs, a smaller circulating current is produced in loop ($JJ_{3} - JJ_{in} - JJ_{2} - JJ_{1}$), which increases the phase of $JJ_{clk}$, acquiring a total phase of $2\pi$. The arrival of an HFQ pulse at the clock input switches the phase of $JJ_{clk}$ to acquire a phase of $2\pi$. Two serial JJs hold the HFQ pulse within the loop and impose a high impedance on the input current pulse. Once the clock pulse arrives, the phase of $JJ_{in}$ switches to 0 since the current in $JJ_{in}$ is greater than the current in $JJ_{clk}$. Due to $JJ_{in}$ switching, a current pulse propagates towards the output, switching $JJ_{out}$ and generating an HFQ pulse, a logic 1. After $JJ_{in}$ switching, another current pulse is generated, switching $JJ_{in}$ to 0. Another current pulse is generated, switching...

**C. OR Gate**

The proposed OR gate consists of two superconductive loops, each containing a single $2\phi$-JJ and three standard JJs with a single output $2\phi$-JJ below the two loops. A schematic of the OR gate is shown in Fig. 8.

In addition to the OR gate shown in Fig. 8, a JTL stage is also shown, drawn as a dashed line. The last stage JTL in the clock input includes a $2\phi$-JJ, unlike input1 and input2 which are connected by a standard JJ. When an HFQ pulse reaches the clock input without a preceding pulse from input1 or input2, the phase of $JJ_{clk}$ switches by $\pi$. This switching event prevents the pulse from propagating to either of the loops or to the output, producing a logic 0 output. When an HFQ pulse enters input1, the phase of $JJ_{in1}$ switches by $\pi$. After the junction switches, a circulating current is produced in loop ($JJ_{3} - JJ_{in1} - JJ_{2} - JJ_{1}$) to increase the phase of the other JJs until a phase of $2\pi$ is achieved. Two serial JJs hold the HFQ pulse within the loop and impose a high impedance on the input current pulse. Once the clock pulse arrives, the phase of $JJ_{in1}$ switches to 0 since the current in $JJ_{in1}$ is greater than the current in $JJ_{clk}$. Due to $JJ_{in1}$ switching, a current pulse propagates towards the output, switching $JJ_{out}$ and generating an HFQ pulse, a logic 1. After $JJ_{in1}$ switching, the phase of the ($JJ_{3} - JJ_{in1} - JJ_{2} - JJ_{1}$) loop returns to zero. No circulating current exists, and the circuit returns to the initial state. When a symmetric HFQ pulse is passed from input2, the same functionality is achieved at the output. When an HFQ pulse arrives at both inputs, the phase of $JJ_{in1}$ and $JJ_{in2}$ switches by $\pi$. Upon application of a clock input pulse, the clock switches $JJ_{in1}$, which produces a current pulse switching $JJ_{in2}$ to 0. Another current pulse is generated, switching...
IV. EVALUATION OF LATENCY AND ENERGY

The proposed $2\phi$-JJ circuits and logically equivalent RSFQ circuits have been simulated in Cadence Virtuoso. The RSFQ circuits are from the SUNY RSFQ cell library [17]. For the standard JJ device, Whiteley Research open source Verilog-A code is used [18]. The $2\phi$-JJ circuits are modeled by revised Verilog-A code which behaves according to (6). A comparison between the proposed $\pi$ circuits and conventional RSFQ circuits is listed in Table I. The critical current for the $2\phi$-JJs ranges between 100 $\mu$A and 220 $\mu$A, and for standard JJs between 100 $\mu$A and 250 $\mu$A. This provides a fair comparison between the logic circuits since the energy is linearly dependent on the critical current of the JJ.

A. Latency

Latency is the difference in time between the arrival of an output pulse upon the arrival of an input clock pulse. The latency of a three stage JTL is the difference between the input pulse and output pulse of four $2\phi$-JJ JTLs, as shown in Fig. 4. If the circuit does not produce an output pulse, the latency is undefined and the output does not change. The latency of the proposed $\pi$ gates and logically equivalent RSFQ gates is listed in Table I. The proposed $\pi$-JTL, inverter, and OR gate are faster by 1.72X, 2.25X, and 2.85X, respectively, than the equivalent RSFQ JTL, inverter, and OR gate.

B. Energy

The energy of the circuits is determined by integrating the power consumed by each junction. The results, listed in Table I, are the energy consumed during one clock cycle for different input combinations. The JTL energy is for four junctions, as shown in Fig. 4, since no clock is used. The proposed $\pi$ JTL, inverter, and OR gate are, respectively, 2.12X, 2.6X, and 4.5X more energy efficient than the equivalent RSFQ circuits. A lower critical current for the $2\phi$-JJ circuits would further improve the energy efficiency.

V. CONCLUSIONS

$2\phi$-JJ logic eliminates the need for inductors, improving the inherent scalability of superconductive circuits. $2\phi$-JJs also enable HFQ data transmission and storage rather than SFQ for greater energy efficiency. The logic state is represented as an HFQ pulse rather than an SFQ pulse, saving energy. The first work to propose superconductive logic circuits based on this innovative $2\phi$-JJ technology with HFQ pulses is presented in this paper. Simulations show that the proposed $\pi$ logic gates are 2.25X faster and require 2.6X less energy as compared to conventional RSFQ logic circuits. Further investigation into $2\phi$-JJ devices and circuits is necessary to enhance the scalability, speed, and energy of superconductive digital systems.
REFERENCES


