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Optimum wire sizing of *RLC* interconnect with repeaters

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Abstract

Repeaters are often used to drive high impedance interconnects. These lines have become highly inductive and can affect signal behavior. The line inductance should therefore be considered in determining the optimum number and size of the repeaters driving a line. The optimum repeater system uses uniform repeater insertion in order to achieve the minimum propagation delay. A tradeoff exists, however, between the transient power dissipation and the minimum propagation delay in sizing long interconnects driven by the optimum repeater system. Optimizing the line width to achieve the minimum power delay product, however, can satisfy current high speed, low-power design objectives. A reduction in power of 65% and delay of 97% is achieved for an example repeater system.

The Power-Delay-Area-Product (PDAP) criterion is introduced as an efficient technique to size the interconnect within a repeater system. A reduction in buffer area of 67% and interconnect area of 46% is achieved based on the PDAP.

Keywords: On-chip inductance; Repeater insertion; Propagation delay; Transient power dissipation; Power delay product; Wire sizing

1. Introduction

Interconnect design has become a dominant issue in high-speed integrated circuits (ICs). With the decreased feature size of CMOS circuits, on-chip interconnect now dominates both circuit delay and power dissipation. Many algorithms have been proposed to determine the optimum wire size that minimizes a cost function such as the delay [1].

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The number of long interconnects doubles every three years [2], further increasing the importance of on-chip interconnect. The behavior of inductive interconnect can no longer be neglected, particularly in long, low-resistance interconnect lines [3]. As on-chip inductance becomes important, some wire optimization algorithms have been enhanced to consider *RLC* impedances [4]. Previous work has not considered the effect of the interconnect width on the repeater insertion process for long inductive lines.

Uniform repeater insertion is an effective technique for driving long interconnects. Based on a distributed *RC* interconnect model, a repeater insertion technique to minimize signal propagation delay was introduced in [5]. A uniform repeater structure decreases the total delay as compared to a tapered buffer structure when driving long resistive interconnects while buffer tapering is more efficient for driving large capacitive loads [6,7]. Different techniques have been developed to enhance the model of a repeater system that considers a variety of design factors [8–14]. The drain/source capacitance of each repeater and multistage repeaters are considered in [15]. Noise aware techniques for repeater insertion and wire sizing have been described in [16–19]. In [20–22], signal integrity, interconnect reliability, and manufacturability issues are discussed.

The work described in [23] assumes that increasing the interconnect width while maintaining the thickness, spacing, and height from the substrate does not reduce the signal delay since the resistance decreases and the capacitance increases. This assumption is not accurate. Different factors affect the total delay such as the coupling capacitance, the driver size, and the load capacitance. Furthermore, with increasing inductive impedances, trends in the propagation delay with changing line width depend upon the number of repeaters and the size of the inserted repeaters.

For an *RC* line, repeater insertion outperforms wire sizing [24]. It is shown in this paper that this behavior is not the case for an *RLC* line. The minimum signal propagation delay always decreases with increasing line width for *RLC* lines if an optimum repeater system is used.

With increasing demand for low-power ICs, different strategies have been developed to minimize power in the repeater insertion process. Power dissipation and area overhead have been considered in previous work [25–30]. The line inductance, however, has yet to be considered in the optimization process of sizing a wire driven by a repeater system. As shown in Fig. 1, the

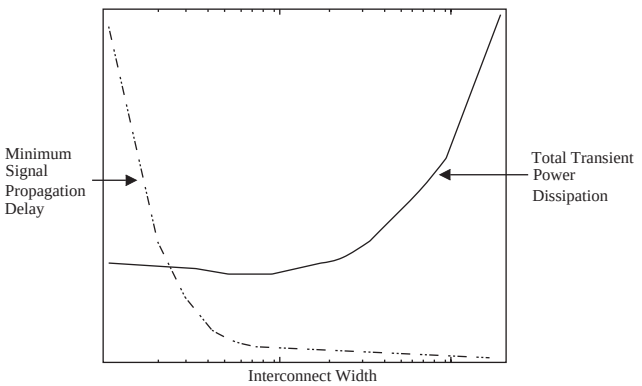

Fig. 1. Minimum signal propagation delay and transient power dissipation as a function of line width for a repeater system.

minimum delay for a signal to propagate along an *RLC* line decreases while the power dissipation increases for wider interconnect [31].

In this paper, the tradeoff between signal propagation delay and transient power dissipation in sizing a long interconnect driven by a repeater system is discussed. Both line inductance and short-circuit power are considered. The minimum power delay product is used as a criterion to size long interconnects. A new criterion, the Power-Delay-Area-Product (PDAP), is introduced as an efficient criterion to size interconnect within a repeater system.

The paper is organized as follows. In Section 2, an overview of a repeater system is presented. The minimum signal propagation delay as a function of interconnect width is described in Section 3. In Section 4, the dependence of the transient power dissipation on wire size is discussed. The area of a repeater system is characterized in Section 5. In Section 6, different criteria to size an interconnect within a repeater system are presented. These criteria are applied to different example circuits in Section 7. Some conclusions are provided in Section 8. In the Appendix, closed-form expressions for the line impedance parameters of a shielded interconnect line are provided.

2. Overview of the repeater insertion process

The primary objective of a uniform repeater insertion system is to minimize the time for a signal to propagate through a long interconnect. Uniform repeater insertion techniques divide the interconnect into equal sections and employ equal size repeaters to drive each section as shown in Fig. 2. In some practical situations, the optimum location of the repeaters cannot be achieved due to physical space constraints. Changing the repeater size can compensate for a change in the ideal physical placement. Bakoglu and Meindl have developed closed-form expressions for the optimum number and size of repeaters to achieve the minimum signal propagation delay in an *RC* interconnect [5]. Adler and Friedman characterized a timing model for a CMOS inverter driving an *RC* load [32,33]. They used this model to enhance the accuracy of the repeater insertion process in *RC* interconnects. Alpert considered the interconnect width as a design parameter [24]. He showed that, for *RC* lines, repeater insertion outperforms wire sizing.

The delay can be greatly affected by the line inductance, particularly low-resistance materials with fast signal transitions. Ismail and Friedman extended previous research in repeater insertion by considering the line inductance [34]. They showed that on-chip inductance can decrease the delay, area, and power of the repeater insertion process as compared to an *RC* line model [35]. Banerjee and Mehrotra developed an analytic delay model and methodology for inserting repeaters into distributed *RLC* interconnect which demonstrated the importance of including line inductance as technology advances [36–39].

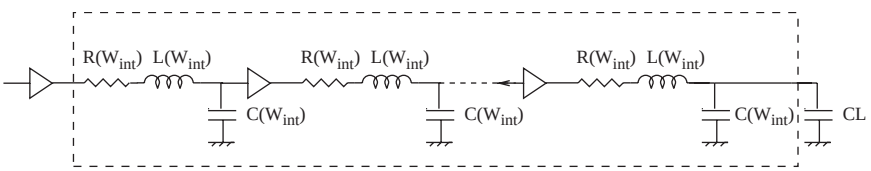

Fig. 2. Uniform repeater system driving a distributed *RLC* interconnect.

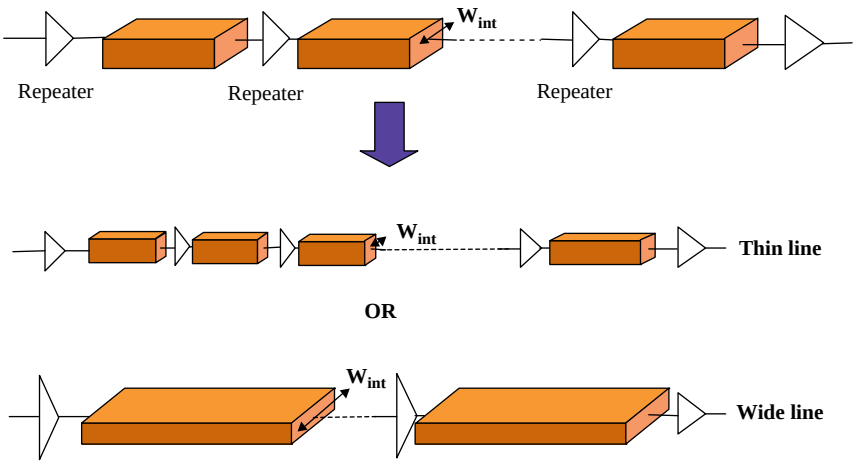

Fig. 3. Wire sizing in a repeater insertion system.

Interconnect sizing within a repeater system affects two primary design parameters, the number of repeaters and the optimum size of each repeater as shown in Fig. 3. Different tradeoffs in sizing long inductive interconnect driven by an optimum repeater system are investigated in this paper. Design criteria are developed to determine the optimum width, while considering different design objectives, such as the delay, power, and area.

3. Propagation delay

The interconnect resistance decreases with increasing line width, increasing L_{int}/R_{int} the ratio between the line inductance and resistance. An increase in L_{int}/R_{int} decreases the number of inserted repeaters to achieve the minimum propagation delay. For an RLC line, the minimum signal propagation delay decreases with wider wires until no repeaters should be used. Wire sizing outperforms repeater insertion in RLC lines.

Expressions for the optimum number of repeaters $k_{opt-RLC}$ and the optimum repeater size $h_{opt-RLC}$ [34] are

$$k_{opt-RLC}(W_{int}) = \sqrt{\frac{R_{int}(W_{int})C_{int}(W_{int})}{2.3R_0C_0}}\frac{1}{\left[1+0.16(T_{L_{int}/R_{int}}(W_{int}))^3\right]^{0.24}}, \tag{1}$$

$$h_{opt-RLC}(W_{int}) = \sqrt{\frac{R_0C_{int}(W_{int})}{R_{int}(W_{int})C_0}}\frac{1}{\left[1+0.16(T_{L_{int}/R_{int}}(W_{int}))^3\right]^{0.3}}, \tag{2}$$

where

$$T_{L_{int}/R_{int}}(W_{int}) = \sqrt{\frac{L_{int}(W_{int})/R_{int}(W_{int})}{R_0C_0}}. \tag{3}$$

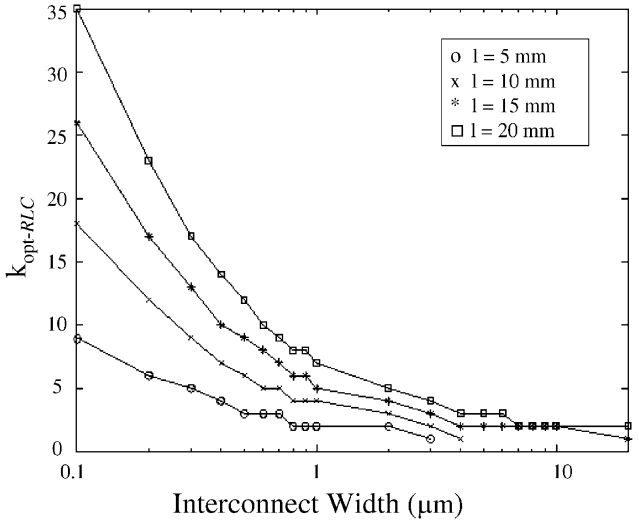

Fig. 4. Optimum number of repeaters for minimum propagation delay for different line widths.

C_0 and R_0 are the input capacitance and output resistance of a minimum size repeater, respectively. $R_{int}(W_{int})$, $C_{int}(W_{int})$, and $L_{int}(W_{int})$ are the interconnect line resistance, capacitance, and inductance as functions of the interconnect width. Closed-form expressions for the line impedance parameters as functions of the interconnect width are provided in the Appendix.

For a copper interconnect line, low κ dielectric material, $R_0 = 2\,\text{k}\Omega$, and $C_0 = 1\text{fF}$, $k_{opt-RLC}$ is determined from (1). For different line lengths l, the optimum number of repeaters $k_{opt-RLC}$ is illustrated in Fig. 4. It is shown in the figure that for an *RLC* line, the optimum number of repeaters which minimizes the signal propagation delay decreases with an increase in the line width for all line lengths. The number of repeaters reaches zero (or only one driver at the beginning of the line) for an interconnect width = 3 μm and 4 μm for $l = 5\,\text{mm}$ and 10 mm, respectively. For widths greater than 4 μm, the wire should be treated as one segment. A repeater system should not be used above a certain width for each line length.

The line capacitance per unit length increases with line width. As the number of inserted repeaters decreases with wider lines, a longer line section is driven by each repeater. An increase in the section length and width increases the capacitance driven by each repeater. To drive a high capacitive load, a larger repeater size is required to decrease the overall delay. As shown in Fig. 5, the optimum repeater size $h_{opt-RLC}$ is an increasing function of line width.

The minimum signal propagation delay of an optimum repeater system decreases with increasing line width as the total gate delay decreases. For an inductive interconnect line, the total signal propagation delay is

$$t_{pd-total}(W_{int}) = k_{opt-RLC}(W_{int}) t_{pd-\text{section}}(W_{int}), \tag{4}$$

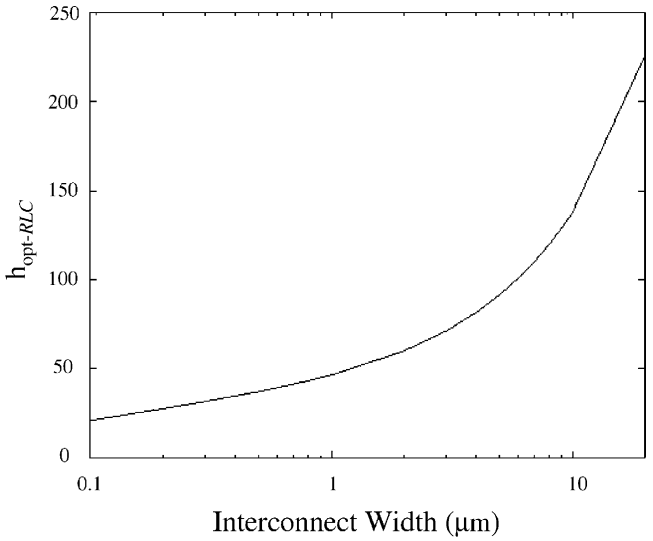

Fig. 5. Optimum repeater size for minimum propagation delay for different line widths.

where $t_{pd\text{-}section}(W_{int})$ is the signal delay of each RLC section as a function of the interconnect width.

$$t_{pd-\text{section}}(W_{int}) = \frac{e^{-2.9\varsigma^{1.35}}}{\omega_n} + 0.74(R_{tr}(W_{int})C_{section}(W_{int}) + R_{section}(W_{int})C_L(W_{int}) + R_{tr}(W_{int})C_L(W_{int}) + 0.5R_{section}(W_{int})C_{section}(W_{int})), \tag{5}$$

where

$$\varsigma = \frac{\omega_n}{2}(0.5C_{section}(W_{int})R_{section}(W_{int}) + C_{section}(W_{int})R_{tr}(W_{int}) + C_L(W_{int})(R_{section}(W_{int}) + R_{tr}(W_{int}))), \tag{6}$$

$$\omega_n = \frac{1}{\sqrt{L_{section}(W_{int})(C_{section}(W_{int}) + C_L(W_{int}))}}, \tag{7}$$

$$C_L(W_{int}) = C_{section}(W_{int}) + h_{opt-RLC}(W_{int})C_0, \tag{8}$$

$$R_{tr}(W_{int}) = \frac{R_0(W_{int})}{h_{opt-RLC}(W_{int})}, \tag{9}$$

$$R_{section}(W_{int}) = \frac{R_{line}(W_{int})}{k_{opt-RLC}(W_{int})}, \tag{10}$$

$$L_{section}(W_{int}) = \frac{L_{line}(W_{int})}{k_{opt-RLC}(W_{int})}, \tag{11}$$

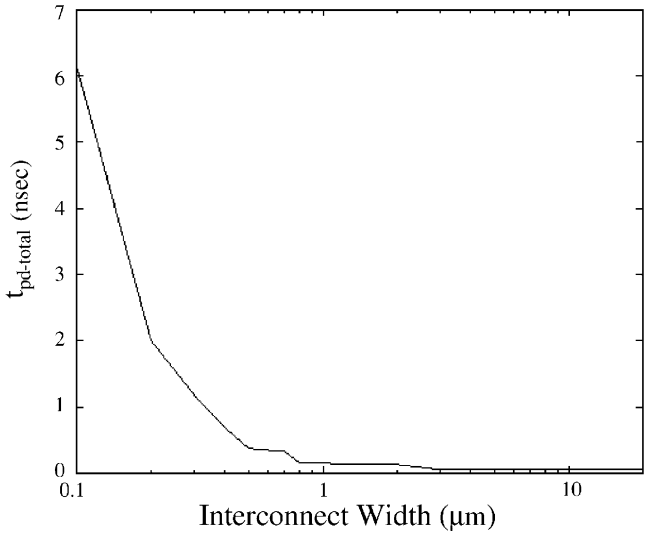

Fig. 6. Minimum signal propagation delay as a function of interconnect width ($l = 5$ mm).

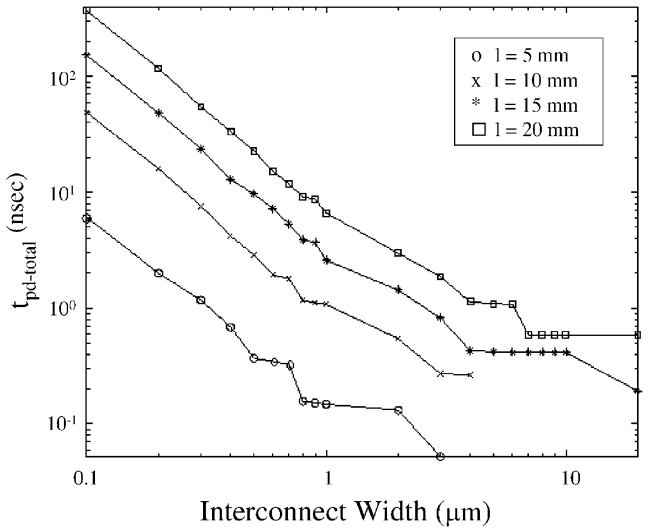

Fig. 7. Minimum signal delay as a function of interconnect width for different line lengths.

$$C_{section}(W_{int}) = \frac{C_{line}(W_{int})}{k_{opt-RLC}(W_{int})}. \tag{12}$$

The minimum delay [obtained from (4)] is shown in Fig. 6 as a function of interconnect width. An increase in the inductive behavior of the line and a reduction in the number of repeaters decrease the minimum signal propagation delay that can be achieved by a repeater system.

The signal delay for different line lengths is shown in Fig. 7. The lower limit in the propagation delay decreases with increasing line width until the number of repeaters is zero. For a system of

repeaters, there is no optimum width at which the total propagation delay is minimum. Rather, the delay is a continuously decreasing function of line width. The propagation delay with no repeaters in an *RLC* line produces a smaller signal propagation delay than using any number of repeaters with any repeater size. For *RLC* interconnect, wire sizing outperforms repeater insertion, producing a smaller signal propagation delay. This characteristic is an important trend when developing a wire sizing methodology for a repeater system.

4. Power dissipation

The power characteristics of a repeater insertion system is discussed in this section. The work described in [25–30] considers power and area as design constraints. The line inductance, however, has not been considered. In Section 4.1, the factors that affect the short-circuit power while considering the line inductance of an interconnect driven by a repeater system is discussed. The dependence of the dynamic power on wire size is described in Section 4.2. The total transient power dissipation characteristics are summarized in Section 4.3.

4.1. Short-circuit power dissipation

Short-circuit current flows when both transistors within an inverting repeater are simultaneously on. Thin lines cause less dynamic power and higher short-circuit power to be dissipated. For thin resistive lines, the number of repeaters can be large. The short-circuit power dissipation in all repeaters along a line is considered. Short-circuit power depends on both the input signal transition time and the load characteristics. A simple and accurate expression for the short-circuit power dissipation of a repeater driving an *RC* load has been presented in [32]

$$P_{sc-section} = \tfrac{1}{2} I_{peak} t_{base} v_{dd} f, \tag{13}$$

where I_{peak} is the peak current that flows from V_{dd} to ground, t_{base} is the time period during which both transistors are on, V_{dd} is the supply voltage, and f is the switching frequency.

Tang used this expression to characterize the short-circuit power of an *RLC* load [40]. A closed form expression for the signal transition time at the far end of an *RLC* line has been described in [41–43]. Increasing the line width has two competing effects on the short-circuit power. As described in [43], the short-circuit power decreases when a line is underdamped. For wide interconnect, the short-circuit power increases as the line capacitance becomes dominant. Furthermore, increasing the length of the section by reducing the number of repeaters increases the short-circuit power of each section due to the higher section impedance.

The total short-circuit power of a repeater system is

$$P_{sc-total} = k_{opt-RLC} P_{sc-section}. \tag{14}$$

Eq. (14) is used in Section 4.3 to characterize the power dissipation in terms of the interconnect width.

4.2. Dynamic power dissipation

The dynamic power is the power required to charge and discharge the various device and interconnect capacitances. The total dynamic power is the summation of the CV^2f power from the line capacitance and the repeaters.

$$P_{dyn-total} = P_{dyn-line} + P_{dyn-repeaters}, \tag{15}$$

where

$$P_{dyn-repeaters} = k_{opt-RLC} h_{opt-RLC} C_0 V_{dd}^2 f, \tag{16}$$

$$P_{dyn-line} = C_{int} V_{dd}^2 f, \tag{17}$$

$P_{\text{dyn-repeaters}}$ depends on both the number and size of each repeater. While the number of repeaters decreases, the repeater size increases.

The dynamic power dissipated by a line increases with greater line capacitance (as the line width is increased). The dynamic power of the repeaters, however, decreases since fewer repeaters are used with wider lines. As shown in Fig. 8, the total dynamic power is a minimum for thin interconnect. The effect of sizing the interconnect on the total transient power dissipation is discussed in Section 4.3.

4.3. Total power dissipation

In order to develop an appropriate criterion for determining the optimal interconnect width between repeaters, the total transient power dissipation of a system needs to be characterized. The total transient power can be described as

$$P_{total}(W_{int}) = V_{dd} f[k_{opt-RLC}(W_{int})(\tfrac{1}{2} I_{peak}(W_{int}) t_{base}(W_{int}) + h_{opt-RLC}(W_{int}) V_{dd} C_0) + V_{dd} C_{int}(W_{int})]. \tag{18}$$

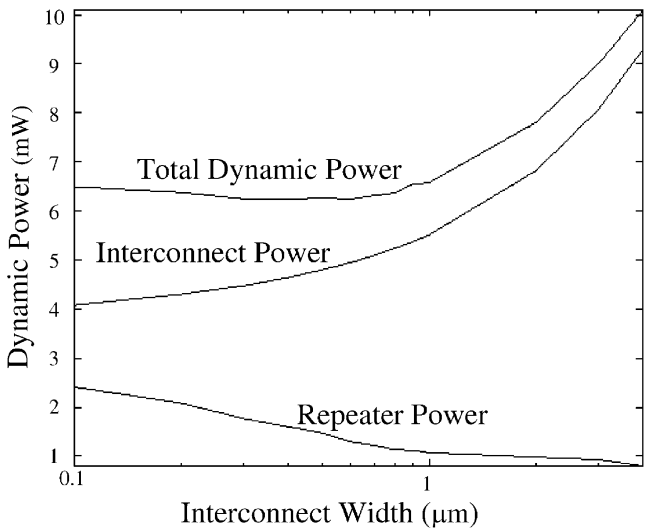

Fig. 8. Dynamic power dissipation as a function of interconnect width for $l = 20$ mm.

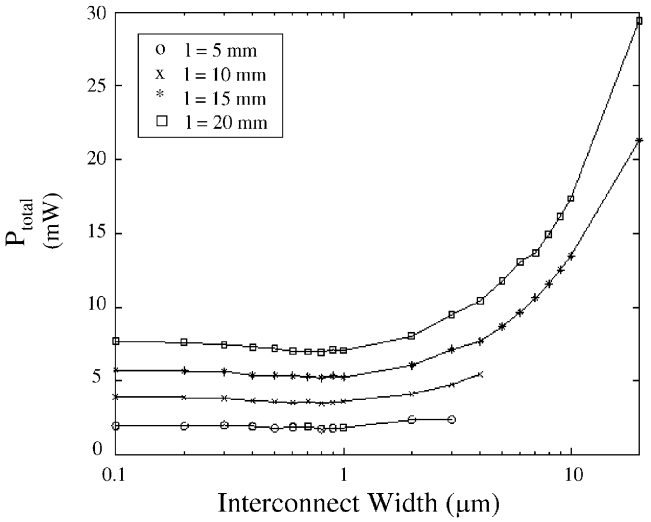

Fig. 9. Total transient power dissipation as a function of interconnect width.

All of the terms in (18) are functions of the line width except V_{dd}, C_0, and f. As described in Sections 4.1 and 4.2, both transient power components decrease with increasing line width, thereby decreasing the total power until the line capacitance becomes dominant.

For an *RLC* interconnect, fewer repeaters are necessary to drive a line while achieving the minimum propagation delay [34]. For an inductive interconnect, the line capacitance is typically larger than the input capacitance of the repeaters. Increasing the width reduces the power dissipation of the repeaters and increases the power dissipation of the line. The reduction in power dissipated by the repeaters overcomes the increase in the interconnect power until the line capacitance dominates the line impedance. After exceeding a certain width, the total power increases with increasing line width.

The total power dissipation as a function of line width for different interconnect lengths is shown in Fig. 9. As the line width increases from the minimum width (i.e., 0.1. μm in the example technology), the total power dissipation is reduced. A minimum transient power dissipation therefore occurs with thin interconnect (see Fig. 9). The minimum transient power dissipation is obtained from

$$\frac{\partial P_{total}}{\partial W_{int}} = 0, \tag{19}$$

where $\partial P_{total}/\partial W_{int}$ is a nonlinear function of W_{int}. Numerical methods are used to obtain values of W_{int} for specific interconnect and repeater parameters.

Over a range of practical interconnect width, the total transient power increases as shown in Fig. 9. As the line length increases, the total power dissipation rapidly increases with increasing line width as the interconnect capacitance becomes dominant. In Section 6, the tradeoff between signal delay and power dissipation is considered in the development of a criterion for interconnect sizing.

5. Area of the repeater system

For a specific interconnect width within a repeater system, the optimum number and size of the repeaters can be determined. Previous studies on repeaters have considered the silicon area, ignoring the metal layer resources [25–30]. Long global interconnects are typically wide and require shielding [44–49]. In order to develop appropriate criteria for considering the area overhead, both the transistors and interconnect are need to be characterized [50–52]. The area of the interconnect metal can be described as

$$A_{line}(W_{int}) = W_{int} l. \tag{20}$$

The interconnect metal area is illustrated in Fig. 10 as a function of the interconnect width. For CMOS inverters used as repeaters, the total silicon area of the active repeaters is

$$A_{repeater}(W_{int}) = 3k_{opt-RLC}(W_{int})h_{opt-RLC}(W_{int})L_n^2, \tag{21}$$

where L_n is the feature size. The PMOS transistor of each repeater is assumed to be twice the size of the NMOS transistor to achieve a symmetric transition. For an *RLC* line, fewer repeaters are needed to minimize the propagation delay, reducing the silicon area as shown in Fig. 11.

The active repeaters and the passive interconnects utilize different layers, making the area overhead of both elements independent, particularly for interconnects routed on the upper layers. A weighted product in (22) is used as a criterion to consider both area parameters in sizing the interconnect,

$$A_{product}(W_{int}) = A_{repeater}(W_{int})^{w_r} A_{line}(W_{int})^{w_l}, \tag{22}$$

where w_r and w_l are the weights of the two cost functions.

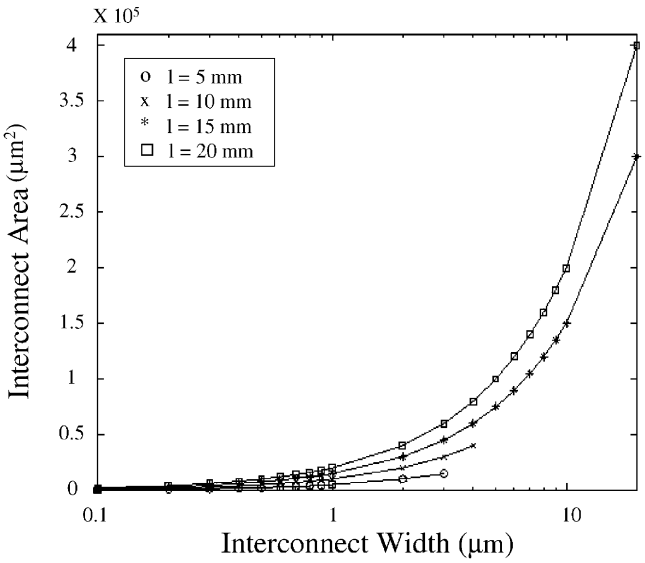

Fig. 10. Interconnect area as a function of interconnect width for different line lengths.

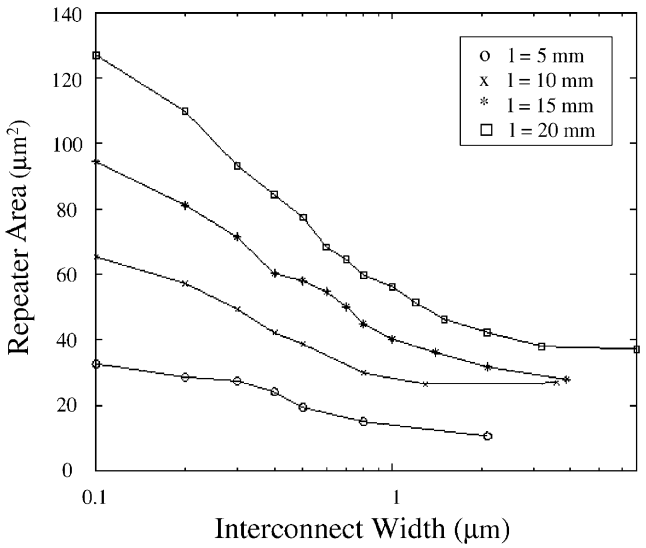

Fig. 11. Total area of the repeaters as a function of the interconnect width for different line lengths.

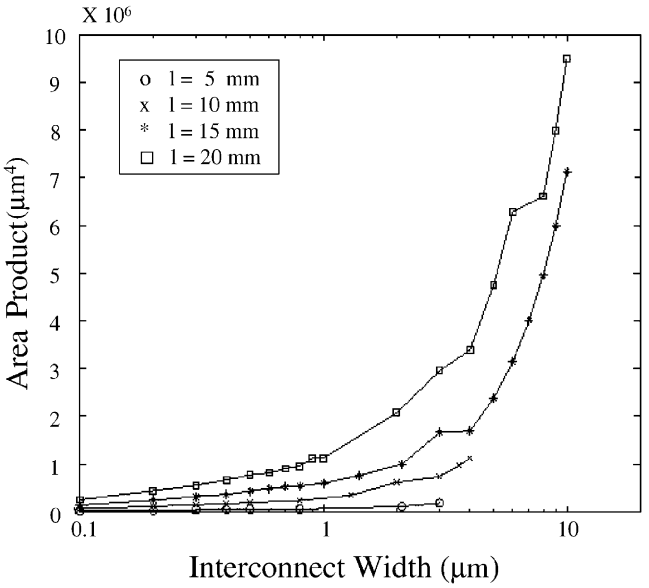

Fig. 12. Product of interconnect and transistor area as a function of the interconnect width for different line lengths.

For $w_r = w_l = 1$, the area product of the system increases with different interconnect widths as shown in Fig. 12. Despite the reduction in repeater area with increasing interconnect width, the increased area occupied by the interconnect increases the overall area of the repeater system. In Section 6, different design criteria are developed to size an interconnect within a repeater system.

6. Design criteria for interconnect within a repeater system

In this section, different design criteria to size interconnect within a repeater system are developed. The optimization criteria have been applied to different repeater systems. The results are summarized in Section 7.

In Section 6.1, a constrained system is considered. Application to an unconstrained system is discussed in Section 6.2.

6.1. Constrained systems

For a constrained system, there is a delay target (minimum speed or maximum delay) and/or a limit on the power dissipation. The minimum signal propagation delay determines a lower limit on the line width while the maximum power dissipation determines the upper limit.

If the minimum limit on the line width obtained from (4) is greater than the maximum width obtained from (18), both limits cannot be simultaneously satisfied and one of the design constrains needs to be relaxed. If the minimum limit is lower than the maximum limit, both constraints can be satisfied.

For a constrained system, the transistor or metal area has an upper limit. The two factors change differently with the width; therefore, there is a tradeoff between the two area components.

6.2. Unconstrained systems

For an *RLC* line, there are four criteria to size interconnect in an unconstrained system. The first criterion is for minimum power while sacrificing speed. The optimum solution for this criterion is obtained from (19).

The second criterion is for minimum delay. As no optimum interconnect width exists for minimum propagation delay, the practical limit is either the maximum repeater size or no repeaters, whichever produces a tighter constraint. The constraint in this case is either the maximum repeater size or the maximum line width. The optimum number of repeaters for a target line width is determined from [34]. If not possible, no repeaters should be used and the design problem reduces to choosing the width of a single section of interconnect [31].

The third and fourth criteria are presented in the following subsections. In Section 6.2.1, the Power-Delay-Product (PDP) as a criterion to size an interconnect within a repeater system is described. The Power-Delay-Area-Product (PDAP) is introduced in Section 6.2.2 as an alternative design criterion.

6.2.1. Power-delay-product design criterion

The PDP criterion satisfies both the power dissipation and speed with no constraints on the area. From the discussions in Sections 2 and 3, the minimum signal propagation delay of an *RLC* interconnect driven by a repeater system decreases with increasing line width. Alternatively, the total transient power has a global minimum at a narrow width. Over the entire range of line width, the total transient power increases with increasing line width. At a line width smaller than the line width for minimum power, the power and delay both increase. An upper limit on the line width is reached where the minimum propagation delay of a repeater system is attained. Beyond that limit,

a single segment sizing criterion should be used to optimize the width according to a cost function (i.e., delay [1] or power [41–43]). Between these two limits, a tradeoff exists between the power dissipation and signal propagation delay. A single expression for the Power-Delay-Product (PDP) as a function of the interconnect width is

$$PDP(W_{int}) = P_{total}(W_{int})^{w_p} t_{pd-total}(W_{int})^{w_d}, \tag{23}$$

where w_p and w_d are the weights of the cost functions. A local minimum for the PDP exists for each line length. The minimum power delay product is obtained by numerically solving the nonlinear equation,

$$\frac{\partial PDP}{\partial W_{int}} = 0. \tag{24}$$

The weights w_p and w_d describe which design objective is more highly valued.

6.2.2. Power-delay-area-product design criterion

The criterion described in Section 6.2.1 does not include the area of the system as a design parameter. In order to include the area of the system, the PDAP criterion is introduced. This criterion satisfies both the power dissipation and speed while considering area. The Power-Delay-Area-Product (PDAP) can be used as a criterion to size the interconnect. A single expression for the PDAP as a function of the interconnect width is

$$PDP(W_{int}) = P_{total}(W_{int})^{w_p} t_{pd-total}(W_{int})^{w_d} A_{repeater}(W_{int})^{w_r} A_{line}(W_{int})^{w_l}. \tag{25}$$

A local minimum for the PDAP exists for each line length. The minimum PDAP is obtained by numerically solving the nonlinear equation,

$$\frac{\partial PDP}{\partial W_{int}} = 0. \tag{26}$$

In the following section, different criteria are applied to different systems to size the interconnect within a repeater system. Different tradeoffs among the delay, power, and area are discussed.

7. Application of interconnect design methodology

The four criteria are applied to a 0.24 μm CMOS technology to determine the optimum solution for different line lengths. No limit on the maximum buffer size is assumed. In order to characterize the line inductance in terms of the geometric dimensions, an interconnect line shielded by two ground lines is assumed. An interconnect line with resistance per square $R_{\square} = 25\,\mathrm{m\Omega/\square}$, capacitance per unit length for minimum width $C_{Wmin} = 66\,\mathrm{fF/mm}$, and inductance per unit length for minimum width $L_{Wmin} = 1\,\mathrm{nH/mm}$ is used. For a repeater system with the following characteristics, $C_0 = 1\,\mathrm{fF}$ and $w_p = w_d = 1$, the optimum solution for each criterion is listed in Table 1. A clock signal with a 20 ps transition time ramp input signal and 250 MHz frequency is used to determine the propagation delay and power dissipation.

The optimum line width for each design criterion is listed in the first row for each line length. The optimum number and size of the repeaters for each line width is listed in the second and third

Table 1
Uniform repeater system for different optimization criteria

	Minimum power	No repeaters	Minimum PDP
$l = 5$ mm:			
W_{int} (μm)	0.8	2.1	2.1
Number of repeaters	1	0	0
Repeater size (of minimum)	43.3	61.2	61.2
Minimum delay (ns)			
Total	0.157	0.051	0.051
Increase (times)	2	1	1
Power (mW)			
Total	1.73	1.98	1.98
Increase (%)	0%	14.5%	14.5%
$l = 15$ mm:			
W_{int} (μm)	0.8	20	3.9
Number of repeaters	5	0	1
Repeater Size (of minimum)	43.2	225.6	80.7
Minimum delay (ns)			
Total	3.87	0.19	0.43
Increase (times)	19.36	1	1.26
Power (mW)			
Total	5.2	21.31	7.58
Increase (%)	0%	310%	45.7%

row of each line length. The per cent increase in the minimum propagation delay based on the optimum power and PDP as compared to no repeaters is also listed. The per cent increase in the total transient power dissipation is provided.

For an $l = 5$ mm line, the optimum interconnect width for both minimum PDP and no repeaters is the same, producing a 14.5% increase in power as compared to the optimum width for minimum power and a reduction of 68% as compared to the optimum width for minimum signal propagation delay.

For short interconnects, few repeaters are necessary to produce the minimum propagation delay. For longer interconnect, an increase in the line capacitance rapidly increases the power dissipation, while the minimum propagation delay decreases more slowly.

For $l = 15$ mm, the optimum solution that minimizes PDP increases the delay by 1.26 rather than 20 times for the solution for minimum power. The power increases by 45% rather than 3.1 times for the no repeater solution. Optimizing the interconnect to produce the minimum power delay produces a smaller increase in both the power and delay as compared to separately optimizing either the power or delay. A reduction in the minimum propagation delay of 89% and in the power dissipation of 65% is achieved if the optimum width for the minimum PDP is used rather than the optimum width for either minimum power or no repeaters.

In order to consider the area of a repeater system, the PDAP criterion is used to size the interconnect. For $w_l = w_r = 1$, the minimum interconnect width is determined from the optimum solution for the minimum area product. The optimum solution for each criterion is listed Table 2.

Table 2
Uniform repeater system for different optimization criteria

	Minimum width	Minimum PDP	Minimum PDAP
$l = 5$ mm:			
W_{int} (μm)	0.1	2.1	2.1
Number of repeaters	8	0	0
Repeater size (of minimum)	21.0	61.2	61.2
Minimum delay (ns)			
Total	0.52	0.051	0.051
Reduction (%)	0%	90.2%	90.2%
Power (mW)			
Total	2.3	1.98	1.98
Reduction (%)	0%	14%	14%
Interconnect area (μm^2)	500	10500	10500
Increase (times)	1	21	21
Silicon area (μm^2)			
Total	33	11	11
Reduction (%)	0%	66.7%	66.7%
$l = 15$ mm:			
W_{int} (μm)	0.1	3.9	2.1
Number of repeaters	25	1	2
Repeater size (of minimum)	21.0	80.7	61.2
Minimum delay (ns)			
Total	2.2	0.43	0.44
Reduction (%)	0%	80.5%	80.5%
Power (mW)			
Total	8.26	7.58	6.34
Reduction (%)	0%	8.2%	23.2%
Interconnect area (μm^2)	1500	58500	31500
Increase (times)	1	39	21
Silicon area (μm^2)			
Total	94	28	32
Reduction (%)	0%	70.2%	66.0%

For an $l = 5$ mm, the optimum interconnect width for both minimum PDP and PDAP is the same, producing the same reduction in delay and increase in power as compared to the criteria listed in Table 1. However, both design objectives (delay and power) are decreased as compared to the minimum width. A reduction in delay of 90% and total power dissipation of 14% is achieved when the PDAP criterion is used. Furthermore, the transistor area is decreased by 67% while the interconnect uses more metal resources.

For $l = 15$ mm, a design based on the minimum PDAP criterion dissipates more power as compared to a design based on the PDP criterion. A reduction in power of 23% is achieved with a negligible increase in the propagation delay. Moreover, the interconnect area decreases from 39 times to 21 times the area of the minimum width, achieving a reduction of 46% in the metal area occupied by the interconnect line. As the interconnect line length increases, the PDAP criterion becomes more efficient if area is considered in the optimization process.

8. Conclusions

Repeater insertion outperforms wire sizing in *RC* lines. However, for *RLC* lines the minimum signal propagation delay always decreases with increasing wire width if an optimum repeater system is used. In *RLC* lines, wire sizing outperforms repeater insertion as the minimum signal propagation delay with the optimum width using no repeaters along the line is less than the minimum signal propagation delay using any number of repeaters. The minimum signal propagation delay always decreases with wider lines until the number of repeaters equals zero. In *RLC* lines, there is no optimum interconnect width for minimum signal propagation delay.

The total transient power dissipation of a repeater system driving an *RLC* line is minimum at small line widths. Below the width for minimum power, both the signal delay and the power dissipation increase. Increasing the line width above the width for minimum power reduces the number of repeaters and the minimum signal propagation delay while increasing the total transient power dissipation. A tradeoff between the transient power dissipation and the signal propagation delay, therefore, exists in sizing the interconnect width.

Optimizing the interconnect for minimum power delay product produces a much smaller increase in both the power and delay as compared to separately optimizing for either the power or delay. As the interconnects become longer, the difference between the optimum width for minimum power and the optimum width for minimum delay increases, further enhancing the effectiveness of the proposed criterion. A reduction in power of 65% and minimum delay of 97% is achieved for an example repeater system driving a long interconnect.

A criterion, Power-Delay-Area-Product (PDAP), is introduced as an efficient technique to size an interconnect within a repeater system if the system area is considered in the design process. A greater reduction in power dissipation of around 23% is achieved with a negligible increase in propagation delay if the line width is optimized for minimum PDAP rather than minimum PDP. Furthermore, a reduction in transistor area of 67% and metal area of 46% is achieved if the PDAP criterion is used.

Appendix A. Expressions for line impedance parameters of an interconnect shielded with two ground lines

For an interconnect line shielded with two ground lines, analytic expressions for the line impedance can be characterized. Closed form expressions for the interconnect resistance, capacitance, and inductance are provided in this appendix. Neglecting skin and proximity effects, the line resistance is characterized by the simple relation,

$$R_{line} = \frac{\rho l}{W_{INT} T}, \tag{A.1}$$

where ρ and T are the line resistivity and thickness, respectively. The line capacitance is [53]

$$C_{int} = \varepsilon_{ox} l (C_a + 2C_b), \tag{A.2}$$

where

$$C_a = \frac{W_{int}}{H} + 2.24\left(\frac{W_{int}}{H}\right)^{0.0275}(1 - 0.85e^{(-0.62\frac{S}{H})}) + 0.32\log\left(\frac{T}{S}\right)(0.15\frac{S}{H}e^{-1.62\frac{T}{S}} - 0.12e^{(-0.065\frac{S}{T})}), \tag{A.3}$$

$$C_b = \frac{T}{S} + 1.31\left(\frac{T}{H}\right)^{0.073}\left(\frac{S}{H} + 1.38\right)^{-2.22} + 0.4\log\left(1 + 5.46\frac{W_{int}}{S}\right)\left(\frac{S}{H} + 1.12\right)^{-0.81}. \tag{A.4}$$

S is the spacing between the signal line and the ground shield and H is the height of the metal layer from the substrate. Assuming the return path is an adjacent ground lines [54], the line inductance is

$$L_{int} = l\left(L_s - 2.0M_{sg} + \frac{L_g}{2.0} + \frac{M_{gg}}{2.0}\right), \tag{A.5}$$

$$L_g = 0.2\left(\log\left(\frac{2l}{W_g + T}\right) + 0.5 + 0.22\frac{W_g + T}{l}\right), \tag{A.6}$$

$$M_{sg} = 0.2\left(\log\left(\frac{2l}{d_{sg}}\right) - 1.0 + \frac{d_{sg}}{l}\right), \tag{A.7}$$

$$M_{gg} = 0.2\left(\log\left(\frac{2l}{d_{gg}}\right) - 1.0 + \frac{d_{gg}}{l}\right), \tag{A.8}$$

$$L_g = 0.2\left(\log\left(\frac{2l}{W_{int} + T}\right) + 0.5 + 0.22\frac{W_{int} + T}{l}\right),$$

where W_g is the width of the ground shield, d_{sg} is the distance between the center of the signal line and the ground shield, and d_{gg} is the distance between the center of the two ground shields.

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