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INDUCTANCE EFFECTS IN RLC TREES

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A closed form solution for characterizing voltage-based signals in an RLC tree is presented. The closed form solution is used to derive figures of merit to characterize the effects of inductance at a specific node in an RLC tree. The *effective* damping factor of the signal at a specific node in an RLC tree is shown to be one useful figure of merit. It is shown that as the effective damping factor of a signal increases, an RC model is sufficiently accurate to characterize the waveform. The rise time of the input signal driving an RLC tree is shown to be a second factor that affects the relative significance of inductance. As the rise time of the input signal increases as compared to the effective LC time constant at a specific node within an RLC tree, the signal at this node will no longer exhibit the effects of inductance. It is demonstrated that a single line analysis to determine the importance of including inductance to characterize an interconnect line that is a part of a tree is invalid in many cases and can lead to erroneous conclusions. The error exhibited by single line analysis is due to the large interaction among the branches of the tree.

Keywords: Inductance; interconnect; damping factor; RLC tree; moments.

1. Introduction

It has become well accepted that interconnect delay dominates gate delay in current deep submicrometer VLSI circuits.¹⁻⁴ With the continuous scaling of technology and increased die area, this situation is expected to become worse. In order to properly design complex circuits, more accurate interconnect models and signal propagation characterization are required. Historically, interconnect has been modeled as a single lumped capacitance in the analysis of the performance of on-chip interconnects. With the scaling of technology and increased chip size, the crosssectional area of wires has scaled down while interconnect length has increased. The

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resistance of the interconnect has therefore become significant, requiring more accurate RC delay models. At first interconnect was modeled as a lumped RC circuit. To further improve accuracy, the interconnect has been modeled as a distributed RC circuit (multiple T or II sections) for those nets requiring more accurate delay models. A well known method used to determine which nets require more accurate delay models is to compare the driver resistance R_{tr} and the load capacitance C_L to the total resistance and capacitance of the interconnect line, R_t and C_t .^{5,6} Typically, those nets that require more accurate RC models are longer, more highly resistive nets.

Currently, inductance is becoming increasingly important with faster on-chip rise times and longer wire lengths. Wide wires are frequently encountered in clock distribution networks and in upper metal layers. These wires are low resistive lines that can exhibit significant inductive effects. Furthermore, performance requirements are pushing the introduction of new materials for low resistance interconnect⁷ and new dielectrics to reduce interconnect capacitance. These technological advances significantly reduce the RC time constants of the interconnect, which increases the effects of inductance.

Inductance, however, need not be included in every net in a VLSI circuit since an RLC model will add to the computational complexity of the circuit simulator with potentially an insignificant gain in accuracy. Inductance should be included only in those nets that exhibit significant inductive effects and for which an RCmodel would cause unacceptable errors. Thus, it is important to determine which nets within a high speed VLSI circuit exhibit significant inductive effects.

The importance of on-chip inductance for single lines has been characterized in Refs. 8–11. However, the nets in a VLSI chip are often structured as trees rather than as single lines. Also, the clock distribution network, which is common to all synchronous digital circuitry, is typically tree structured. The performance of a VLSI chip heavily depends on the design of the clock distribution network where the most accurate interconnect models are required. It is shown in this paper that the branches of a tree cannot be treated as single lines for the purpose of evaluating inductance effects. Rather, the entire tree should be examined for inductance effects as a single structure since a large interaction occurs among the different branches. It is therefore shown that applying a single line analysis to an RLC tree can cause misleading conclusions.

The focus of this paper is the introduction of simple figures of merit that can be used as criteria to determine which nets (and trees in general) require more accurate RLC models. A second order approximation for a signal at a particular node of an RLC tree is described in Sec. 2. The effective damping factor of a signal at a specific node of a tree and the rise time of the input signal are used to derive two figures of merit that describe the relative importance of inductance for the signal at this node. These figures of merit are presented in Sec. 3. In Sec. 4, examples of RLC trees are used to illustrate the error encountered in treating a branch of a tree as a single line. Finally, some conclusions are offered in Sec. 5.



Fig. 1. Simple *RLC* circuit.

2. Second Order Approximation for *RLC* Trees

A second order transfer function that approximates a higher order transfer function at a specific node of an RLC tree is introduced in this section. Wyatt¹² developed a first order approximation for RC trees based on the Elmore delay¹³ assuming that the system has only one dominant pole. Both Wyatt and Elmore assumed a monotone system, which is not valid for an RLC circuit. For example, consider the single section RLC circuit shown in Fig. 1. This circuit has a second order transfer function given by:

$$g(s) = \frac{1}{s^2 L C + s R C + 1}.$$
 (1)

Note that the coefficient of s^1 is RC, which does not include the inductance L. This characteristic means that the Elmore time constant¹³ (and also Wyatt's approximation¹²) does not depend on inductance. However, inductance can have a significant effect on the transient response of a circuit. To better observe the effects of inductance, the transfer function of the circuit can be rearranged as:

$$g(s) = \frac{\omega_n^2}{s^2 + s^2 \zeta \omega_n + \omega_n^2},$$
(2)

where

$$\zeta = \frac{1}{2} \frac{RC}{\sqrt{LC}} \,, \tag{3}$$

$$\omega_n = \frac{1}{\sqrt{LC}} \,. \tag{4}$$

The poles of the transfer function in terms of the damping factor of the system, ζ , are:

$$P_{1,2} = \omega_n [-\zeta \pm \sqrt{\zeta^2 - 1}].$$
 (5)

Note that if ζ is less than one, the poles are complex and oscillations occur in the response, which violates the monotone condition required by the Elmore delay model. In that case the response is called underdamped and overshoots occur. If ζ is greater than one, the poles are real and the response is called an overdamped response. If ζ is equal to one, the response is called a critically damped response.

Note in Eq. (3) that as the inductance increases, ζ decreases, which violates the assumption of a monotonic response used in both the Elmore and Wyatt delay models.

To characterize a nonmonotonic response, at least a second order approximation is necessary because a nonmonotone response involves complex poles, which appear in conjugate pairs. Thus, a second order system of the form described by Eq. (2) can approximate a system with a nonmonotonic response. Therefore, it is necessary to find a value of ζ and ω_n that makes the second order approximation as accurate as possible as compared to the exact transfer function.

Matching the moments of a transfer function to the moments of a higher order system permits the transfer function to approximate the system.¹⁴⁻¹⁹ If a system has an exact transfer function G(s), the normalized transfer function g(s) is given by G(s)/G(0). An exact normalized transfer function of a system can be expanded in the powers of s as:

$$g(s) = 1 + m_1 s + m_2 s^2 + \cdots, (6)$$

where m_i is the *i*th moment of the transfer function.¹⁹ The moments of a transfer function include information about the poles and zeros of the system. For example, the first moment of the transfer function m_1 is:

$$m_1 = \sum_{i=1}^m \frac{1}{p_i} - \sum_{i=1}^n \frac{1}{z_i},$$
(7)

where p_i and z_i are the poles and zeros of the transfer function, respectively. Thus, if there is only one dominant pole in the system with no low frequency zeros that can cancel the dominant pole, the first moment is sufficient to describe the system and can be treated as the reciprocal of the dominant pole. For example, Wyatt used only the first moment to obtain a first order system to approximate an RCtree.¹² For general systems, several moments can be used to calculate a higher order approximate transfer function that better approximates the system. The greater the number of moments that are matched, the more accurately the transfer function approximates the system. Several numerical methods have been introduced to efficiently calculate the poles and residues of an approximate transfer function of a higher order system.¹⁵⁻¹⁸ One example of these model reduction methods is commonly called asymptotic wave evaluation.¹⁵

Applying the moment matching method, the transfer function in Eq. (2) is expanded in powers of s where the first two moments of the transfer function are equated to the first two moments of the nonmonotonic system, m_1 and m_2 . The expansion of the transfer function in Eq. (2) is:

$$g(s) = 1 - s\left(\frac{2\zeta}{\omega_n}\right) + s^2\left(\frac{-1 + (2\zeta)^2}{\omega_n^2}\right) - \dots = 1 + m_1 s + m_2 s^2 + \dots .$$
(8)

The parameters that characterize the second order approximation of a nonmonotone system, ζ and ω_n , can be calculated in terms of the moments of the nonmonotonic

system and are:

$$\zeta = \frac{-m_1}{2} \frac{1}{\sqrt{m_1^2 - m_2}},\tag{9}$$

$$\omega_n = \frac{1}{\sqrt{m_1^2 - m_2}} \,. \tag{10}$$

Hence, for a system with a nonmonotone response, a second order approximation can be found if the first and second moments of the system are known.

For the general RLC tree shown in Fig. 2, the voltage drop at any node i as compared to the input voltage is:

$$V_{\rm in}(s) - V_i(s) = \sum_k C_k V_k(s) s[R_{ki} + L_{ki}s], \qquad (11)$$

where $R_{ik}(L_{ik})$ is the common resistance (inductance) from the input to nodes iand k. For example, $L_{77} = L_1 + L_3 + L_7$, $L_{67} = L_1 + L_3$, and $L_{27} = L_1$. The summation variable k operates over all the capacitors in the circuit. If the input is a unit impulse, $V_{in}(s)$ is equal to 1.0 and the voltages at the nodes of the tree are



Fig. 2. General *RLC* tree.

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the unit impulse responses of these nodes. Thus, the normalized transfer function $g_i(s)$ at node *i* is given by $V_i(s)$ and is:

$$g_i(s) = 1 - \sum_k C_k V_k(s) s[R_{ki} + L_{ki}s] = 1 + m_1^i s + m_2^i s^2 + \cdots .$$
(12)

The first and second moments of the transfer function at node i can be found from

$$m_1^i = \frac{dg_i(s)}{ds}\Big|_{s=0},\tag{13}$$

$$m_2^i = \frac{1}{2!} \frac{d^2 g_i(s)}{ds^2} \Big|_{s=0}.$$
 (14)

Differentiating Eq. (12) with respect to s and substituting s = 0,

$$m_1^i = -\sum_k C_k R_{ik} V_k(s)|_{s=0} , \qquad (15)$$

$$m_2^i = -\sum_k C_k R_{ik} \frac{dV_k(s)}{ds} \bigg|_{s=0} - \sum_k C_k L_{ik} V_k(s) \bigg|_{s=0} \,.$$
(16)

Note that $V_k(s)|_{s=0} = 1$, and that $dV_k(s)/ds|_{s=0} = m_1^k$ since $V_k(s) = g_k(s) = 1 + m_1^k s + m_2^k s^2 + \cdots$. Thus, the first and second moments of a general *RLC* tree at node *i* are:

$$m_1^i = -\sum_k C_k R_{ik} \,, \tag{17}$$

$$m_2^i = \sum_k \sum_j C_k R_{ik} C_j R_{kj} - \sum_k C_k L_{ik} \,.$$
(18)

The first term in m_2^i can be approximated by $(\sum_k C_k R_{ik})^2$. This approximation is particularly accurate for balanced trees. Thus, the second moment of $g_i(s)$ can be approximated by:

$$m_2^i = \left(\sum_k C_k R_{ik}\right)^2 - \sum_k C_k L_{ik} \,. \tag{19}$$

Substituting the first and second moments of a general RLC tree into Eq. (9), ζ_i and ω_{ni} that characterize a second order approximation of the transfer function at node *i* are:

$$\zeta_i = \frac{1}{2} \frac{\sum_k C_k R_{ik}}{\sqrt{\sum_k C_k L_{ik}}},$$
(20)

$$\omega_{ni} = \frac{1}{\sqrt{\sum_{k} C_k L_{ik}}} \,. \tag{21}$$



Fig. 3. AS/X simulations as compared to the second order approximation and the Wyatt model.

Note the similarity between Eqs. (20) and (21) with ζ and ω_n for a single *RLC* section in Eqs. (3) and (4), respectively. The time constants *RC* and \sqrt{LC} are replaced by the summations of equivalent time constants in the tree. Note also that Eqs. (20) and (21) becomes Eqs. (3) and (4), respectively, for a single section. This second order approximation of an *RLC* tree has the same accuracy characteristics as the Wyatt approximation of an *RC* tree.¹²

The second order approximation is compared in Fig. 3 to AS/X^{20} simulations of the output node 7 of the tree shown in Fig. 2. A balanced tree is considered. The supply voltage is 2.5 volts. A step input is applied to both the *RLC* tree and the second order approximation, permitting the transient response at node 7 to be determined. Note the accuracy that the second order approximation exhibits as compared to AS/X simulations for the case of a balanced tree. If the tree is unbalanced, the second order approximation is less accurate. Wyatt's approximation is also shown in Fig. 3. Note that Wyatt's approximation fails to match the response of an *RLC* tree with significant inductance.

3. Effect of Damping Factor and Input Rise Time

A second order approximation of the signals in an RLC tree is used in this section to determine if the signal at a certain node exhibits significant inductance effects. In Sec. 3.1, the effective damping factor ζ_i at node *i* of an RLC tree is used to characterize when an RC model is sufficiently accurate as compared to an RLCmodel, permitting inductance to be neglected. It is shown that as ζ_i increases (or as the equivalent RC time constant at node *i* increases as compared to the equivalent LC time constant), inductance effects decrease. In Sec. 3.2, the effect of the input rise time on the importance of inductance is discussed. It is shown that as the input rise time increases as compared to the equivalent LC time constant at node i, the effect of inductance on the transient behavior of the signal at node i becomes less significant.

3.1. Damping factor

A step signal is used as the input to the second order approximation of the transfer function at node i of an RLC tree to investigate the relationship between the effective damping factor ζ_i and the significance of inductance on the transient behavior of the signal at node i. A step input is used since a step signal eliminates the effect of the rise time and maximizes the significance of the inductance, permitting the effect of the damping factor to be investigated. For a step input and a supply voltage of V_{DD} volts, the signal at node i is:

$$S_{i}(t) = V_{DD} + V_{DD} \\ \times \left[\frac{\exp[\omega_{ni}t(-\zeta_{i} + \sqrt{\zeta_{i}^{2} - 1})]}{-\zeta_{i} + \sqrt{\zeta_{i}^{2} - 1}} - \frac{\exp[\omega_{ni}t(-\zeta_{i} - \sqrt{\zeta_{i}^{2} - 1})]}{-\zeta_{i} - \sqrt{\zeta_{i}^{2} - 1}} \right].$$
(22)

As the damping factor increases, the importance of the inductance on the circuit decreases. Thus, the following approximation can be made assuming large ζ_i ,

$$\sqrt{\zeta_i^2 - 1} \approx \zeta_i \left[1 - \frac{1}{2\zeta_i^2} \right], \quad \text{with a relative error} < \frac{1}{4\zeta_i^4}.$$
(23)

With $\zeta_i > 2.5$, the error due to this approximation is less than 0.7%. With this approximation, the signal at node *i* can be approximated by:

$$S_{i}(t) = V_{DD} + \frac{V_{DD}}{2\left[\zeta_{i} - \frac{1}{2\zeta_{i}}\right]}$$

$$\times \left[-2\zeta_{i} \exp\left[\omega_{ni}t\left(-\frac{1}{2\zeta_{i}}\right)\right] + \frac{\exp\left[\omega_{ni}t\left(-2\zeta_{i} - \frac{1}{2\zeta_{i}}\right)\right]}{2\zeta_{i}}\right]. \quad (24)$$

For $\zeta_i > 2.5$, this expression can be further approximated by:

$$S_i(t) \cong V_{DD} - V_{DD} \exp\left[\omega_{ni} t\left(-\frac{1}{2\zeta_i}\right)\right] = V_{DD} - V_{DD} \exp\left[-\frac{t}{\sum_k C_k R_{ik}}\right], \quad (25)$$

with an error less than 8%. The maximum error is realized when the signal initially switches since the exponential terms are still relatively large. Note that Eq. (25) is precisely Wyatt's approximation for a step response at node *i* of an *RC* tree.¹² This relation shows that for $\zeta_i > 2.5$, the inductance has a minimal effect on the transient response at node i, which is similar to the response of an equivalent RC tree where inductance is neglected. Thus, the first figure of merit presented in this paper is:

$$\zeta_{i} = \frac{1}{2} \frac{\sum_{k} C_{k} R_{ik}}{\sqrt{\sum_{k} C_{k} L_{ik}}} > 2.5.$$
(26)

If this inequality is satisfied, the effects of inductance at node i are negligible. A plot of AS/X²⁰ simulations for the *RLC* tree shown in Fig. 2 at output node 7 as compared to an equivalent tree with all inductances equal to zero is shown in Fig. 4



Fig. 4. Effect of the equivalent damping factor on the accuracy of the RLC and RC models.

for several values of ζ_i . The closed form solution in Eq. (22) is also shown. Note that for $\zeta_i > 2.5$, the response of the *RLC* tree is almost identical to that of an equivalent *RC* tree in which inductance is neglected.

3.2. Input rise time

An exponential signal of the form,

$$V_{\rm in}(t) = V_{DD} \left[1 - \exp\left(-\frac{t}{\tau}\right) \right] u(t) , \qquad (27)$$

is used as the input to the second order approximation of the transfer function of an *RLC* tree to investigate the relationship between the input rise time and the effects of inductance on the transient behavior of the signal at node *i*. u(t) is the unit step function, V_{DD} is the supply voltage, and the 90% rise time of the input signal is 2.3τ where τ is the time constant of the exponential in Eq. (27). With this input signal, the response at node *i* of an *RLC* tree is:

$$e_{i_{RLC}}(t) = V_{DD} \left[1 - k e^{-t/\tau} + \frac{e^{-\zeta_i \omega_{ni} t}}{\sqrt{1 - \zeta_i^2}} \left[\sin(\omega_{ni} t - \theta_1) - \sqrt{\frac{1}{k}} \sin(\omega_{ni} t - \theta_2) \right] \right],$$
(28)

where

$$\theta_1 = \tan^{-1} \left[\frac{\sqrt{1 - \zeta_i^2}}{\zeta_i} \right],\tag{29}$$

$$\theta_2 = \tan^{-1} \left[\frac{\left(\frac{\tau}{T_{LCi}}\right) \sqrt{1 - \zeta_i^2}}{\left(\frac{\tau}{T_{LCi}}\right) \zeta_i - 1} \right],\tag{30}$$

and

$$k = \frac{\left(\frac{\tau}{T_{LCi}}\right)^2}{\left(\frac{\tau}{T_{LCi}}\right)^2 - 2\zeta\left(\frac{\tau}{T_{LCi}}\right) + 1}.$$
(31)

 T_{LCi} is

$$T_{LCi} = \sqrt{\sum_{k} C_k L_{ik}} \,. \tag{32}$$

According to Wyatt's approximation,¹² if the same input is applied to an RC tree, the response at node i is:

$$e_{i_{RC}}(t) = V_{DD}[1 - k_2 e^{-t/\tau} + e^{-t/T_{RCi}}[k_2 - 1]], \qquad (33)$$

where

$$k_2 = \frac{\left(\frac{\tau}{T_{RCi}}\right)}{\left(\frac{\tau}{T_{RCi}}\right) - 1},\tag{34}$$

$$T_{RCi} = \sum_{k} C_k R_{ik} \,. \tag{35}$$

When the rise time of the input signal increases, Eq. (28) approaches Eq. (33). This trend can be better understood by noting that if τ/T_{LCi} and τ/T_{RCi} are both much greater than one, k and k_2 tend to one and θ_2 tends to θ_1 . Thus, if τ/T_{LCi} and τ/T_{RCi} are much greater than one, the response at node i of an RLC tree does not exhibit any effects caused by inductance and an RC tree model can be used to model the interconnect tree. These two conditions, τ/T_{LCi} and τ/T_{Rci} , are much greater than one and reduce to the first condition if the damping factor figure of merit described by Eq. (26) is considered. If ζ_i is greater than 2.5, the inductance effects are not significant because of the damping factor and there is no need to determine the rise time of the input signal. If ζ_i is less than 2.5, then $T_{RCi} < 5T_{LCi}$. Thus, $\tau/T_{LCi} < 5\tau/T_{RCi}$ is the range where the input rise time should be evaluated ($\zeta_i < 2.5$). Hence, if τ/T_{LCi} is much greater than one and $\zeta_i < 2.5$, then τ/T_{RCi} is also much greater than one.

The second figure of merit can be derived by assuming $\tau/T_{LCi} = 10$ and using the relation $t_{rin} = 2.3\tau$. Thus, the second figure of merit is:

$$t_{rin} > 23 \sqrt{\sum_{k} C_k L_{ik}} \,. \tag{36}$$

If this inequality is satisfied, the effects of inductance at node *i* can be neglected. A plot of AS/X^{20} simulations of the *RLC* tree shown in Fig. 2 at output node 7 as compared to an equivalent tree with no inductances is shown in Fig. 5 for several values of t_{rin} . The closed form solution (28) is also shown. ζ_i is maintained constant at 0.5 so that the inductance cannot be ignored. Note that for $t_{rin}/T_{LCi} > 23$, the response of the *RLC* tree is the same as that of an equivalent *RC* tree in which inductance is neglected.

4. Results and Examples

Examples illustrating the importance of using a tree analysis for characterizing inductance effects as well as general traits of inductance effects in RLC trees are presented in this section. In Sec. 4.1, a single line analysis to characterize the importance of inductance is compared to a tree analysis and an example is given that demonstrates a single line analysis can lead to erroneous conclusions. The effect of the size of a tree on the significance of inductance is discussed in Sec. 4.2. It is shown that there is a range of tree size for which inductance effects are prominent.



Fig. 5. Effect of the rise time on the inductance effects in an RLC tree. t_{rin}/T_{LC} is varied from 0.1 to 25. AS/X simulations are shown for an RC tree and an RLC tree. Equation (28) is also shown to illustrate the accuracy of the closed form solution introduced here. Note that as t_{rin}/T_{LC} increases, the RC model approaches the RLC model.

4.1. Tree analysis versus single line analysis

The analysis of single lines to characterize the importance of on-chip inductance has been previously evaluated.^{8–11} However, analyzing single lines to characterize the importance of inductance in RLC trees can be invalid. To illustrate this point, values for the branch resistances, inductances, and capacitances for the RLC tree shown in Fig. 2 are listed in Table 1. According to Refs. 8–11, if a single line analysis is used for each branch, the damping factor for branch *i* is:

$$\zeta_i = \frac{1}{2} \frac{R_i C_i}{\sqrt{L_i C_i}} \,. \tag{37}$$

Branch	$R~(\Omega)$	L (nH)	C (pF)
1	25	10	2
2	50	10	1
3	50	10	1
4	100	0.5	0.5
5	100	0.5	0.5
6	100	0.5	0.5
7	100	0.5	0.5

Table 1. Branch impedances for the RLC tree shown in Fig. 2.

Table 2. Damping factors for the nodes of both the RLC single lines and the RLC tree shown in Fig. 2.

Node	ζ_i (<i>RLC</i> single line analysis)	ζ_i (<i>RLC</i> tree analysis)
1	0.176	0.306
2	0.25	0.441
3	0.25	0.441
4	1.58	0.529
5	1.58	0.529
6	1.58	0.529
7	1.58	0.529

The damping factor of branch *i* affects the signal at node *i*. The single line analysis and the *RLC* tree analysis introduced here are compared in Table 2 for the tree shown in Fig. 2. The branch impedance values listed in Table 1 are used. Note the large difference in the values of the damping factors according to an *RLC* single line analysis as compared to an *RLC* tree analysis. For example, at node 7, the *RLC* single line analysis anticipates no significant inductance effects ($\zeta_7 = 1.58$) while an *RLC* tree analysis anticipates large inductance effects ($\zeta_7 = 0.529$). Simulations of the voltage signal at node 7 of the *RLC* tree shown in Fig. 2 with the branch impedance values listed in Table 1 are shown in Fig. 6. The voltage at node 7 exhibits high inductive effects as anticipated by the *RLC* tree analysis introduced here. This simple example demonstrates that an *RLC* single line analysis can lead in certain cases to erroneous conclusions. Note also that for node 1, the *RLC* single line analysis anticipates greater inductance effects ($\zeta_1 = 0.176$) as compared to the *RLC* tree analysis ($\zeta_1 = 0.306$).

The *RLC* single line analysis generates a significant difference between the maximum and minimum damping factors $(0.176 < \zeta < 1.58)$ as compared to the difference between the maximum and minimum damping factors in the more accurate *RLC* tree analysis $(0.306 < \zeta < 0.529)$. This behavior is due to analyzing each line individually while in reality all of the branches in the tree interact significantly, distributing the effects of the branch inductances throughout the tree. Alternatively, the branches with higher inductive effects and the branches with lower inductance effects influence each other, making the effect of inductance less on those branches



Fig. 6. AS/X simulations of the output voltage at node 7 of the RLC tree shown in Fig. 2 with the branch impedance values listed in Table 1 for the equivalent RC tree.

with higher inductance effects and more on those branches with lower inductance effects. This phenomenon is accurately captured by the RLC tree analysis introduced in this paper.

4.2. Effect of tree size on the significance of inductance

The effect of increasing the size of the tree is to increase the damping factors at the nodes of the tree (and thus decrease the importance of the inductance). If the size of a tree increases, both of the summations $\sum_k C_k R_{ik}$ and $\sum_k C_k L_{ik}$ increase. As described by Eq. (20), ζ_i is half the first summation over the square root of the second summation. Thus, if the two summations increase at the same rate while increasing the size of the tree, the net result is an increase in ζ_i . For example, the damping factor at node 1 for the *RLC* tree shown in Fig. 2 is:

$$\zeta_1 = \frac{1}{2} \frac{R_1 C_T}{\sqrt{L_1 C_T}} = \frac{R_1}{2} \sqrt{\frac{C_T}{L_1}},$$
(38)

where C_T is the total capacitance of the tree. If the size of the tree increases, C_T also increases, making the damping factor at node 1 larger.

An important example of an RLC tree is a tree structured clock distribution network. A clock distribution network is often structured as a balanced tree with a wide trunk and narrowing branches.^{21–23} If a tree has a branching factor of two (where each line is the parent of two other lines), for impedance matching purposes the parent will have double the width of its children.^{22,24,25} The size of the tree can be characterized by the number of levels n. A tree that has n levels has $2^n - 1$ branches. For example, the tree shown in Fig. 2 has three levels and seven branches. The impedance of the branches in each level (r = 1, 2, ..., n) can be approximated



Fig. 7. Effect of the number of levels n on the output damping factor ζ_{out} of a binary clock tree.

by $2^{r-1}R_{\text{root}}$, L_{root} , and $C_{\text{root}}/2^{r-1}$, where R_{root} , L_{root} , and C_{root} are the root resistance, inductance, and capacitance, respectively. The number of branches in level r is 2^{r-1} . Note that the inductance is assumed constant since it is a slowly varying function with the width of the interconnect.^{10,26} The damping factor at an output node can be calculated as a function of the number of levels (representing the size of the tree) and the root impedance and is:

$$\zeta_{\rm out} = \frac{1}{4\sqrt{2}} \frac{R_{\rm root} C_{\rm root}}{\sqrt{L_{\rm root} C_{\rm root}}} \frac{n(n+1)}{\sqrt{2^{-n} + (n-1)}} \,. \tag{39}$$

Note that the output damping factor increases monotonically as n increases. For large n, ζ_{out} increases as $n^{1.5}$. A plot of ζ_{out} versus n is shown in Fig. 7.

Alternatively, if the size of the tree is smaller, the rise time of the input signal can be much greater than T_{LCi} which, according to the second figure of merit in Eq. (36), eliminates the effects of inductance. Thus, there is a range of the size of an *RLC* tree where inductance effects are significant. For the special case of a single *RLC* line, the size is simply represented by the length of the line. This behavior is consistent with the results described in Ref. 11 in which there is a range of interconnect line length where inductance effects are significant.

5. Conclusions

A second order approximation of an RLC tree with the same accuracy characteristics as the Wyatt approximation for an RC tree has been introduced. This second order approximation is used to derive two simple figures of merit to evaluate the significance of the inductance effects exhibited by an RLC tree. The first figure of merit is the damping factor of a signal at a specific node of a tree. It is shown that as the damping factor increases, inductance effects decrease. The second figure of merit is the rise time of the input signal as compared to the effective LCtime constant of the tree at a specific node. It is also shown that as the input rise time increases as compared to the effective LC time constant, the importance of inductance decreases. Evidence is provided that using a single RLC line analysis for those branches within a tree can lead to incorrect conclusions. The error exhibited by a single line analysis is due to the large interaction among the branches of a tree. Finally, it is shown that there is a range of the size of an RLC tree where a tree can exhibit significant inductive effects.

References

- J. M. Rabaey, Digital Integrated Circuits, A Design Perspective, Prentice Hall, Inc., New Jersey, 1996.
- D. A. Priore, "Inductance on silicon for sub-micron CMOS VLSI", Proc. IEEE Symp. VLSI Circuits, May 1993, pp. 17–18.
- D. B. Jarvis, "The effects of interconnections on high-speed logic circuits", *IEEE Trans. Electron. Comput.* EC-10, 4 (1963) 476–487.
- M. P. May, A. Taflove, and J. Baron, "FD–TD modeling of digital signal propagation in 3-D circuits with passive and active loads", *IEEE Trans. Microwave Theory and Techniques* MTT-42, 8 (1994) 1514–1523.
- T. Sakurai, "Approximation of wiring delay in MOSFET LSI", *IEEE J. Solid-State Circuits* SC-18, 4 (1983) 418–426.
- G. Y. Yacoub, H. Pham, and E. G. Friedman, "A system for critical path analysis based on back annotation and distributed interconnect impedance models", *Microelectronic J.* 18, 3 (1988) 21–30.
- J. Torres, "Advanced copper interconnections for silicon CMOS technologies", Appl. Surface Sci. 91, 1 (1995) 112–123.
- A. Deutsch et al., "High-speed signal propagation on lossy transmission lines", IBM J. Res. Development 34, 4 (1990) 601–615.
- A. Deutsch et al., "Modeling and characterization of long interconnections for highperformance microprocessors", IBM J. Res. Development 39, 5 (1995) 547–667.
- A. Deutsch et al., "When are transmission-line effects important for on-chip interconnections?", *IEEE Trans. Microwave Theory and Techniques* MTT-45, 10 (1997) 1836–1846.
- Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Figures of merit to characterize the importance of on-chip inductance", *Proc. IEEE/ACM Design Automation Conf.*, June 1998, pp. 560–565.
- J. L. Wyatt, Circuit Analysis, Simulation and Design, Elsevier Science Publishers, North-Holland, 1987.
- W. C. Elmore, "The transient response of damped linear networks", J. Appl. Phys. 19 (1948) 55–63.
- L. T. Pillage and R. A. Rohrer, "Delay evaluation with lumped linear RLC interconnect circuit models", Proc. Caltech Conf. VLSI, May 1989, pp. 143–158.
- L. T. Pillage and R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis", IEEE Trans. Computer-Aided Design CAD-9, 4 (1990) 352–366.
- C. L. Ratzlaff, N. Gopal, and L. T. Pillage, "RICE: Rapid Interconnect Circuit Evaluator", Proc. IEEE/ACM Design Automation Conf., June 1991, pp. 555–560.

- T. K. Tang and M. S. Nakhla, "Analysis of high-speed VLSI interconnects using the asymptotic waveform evaluation techniques", *IEEE Trans. Computer-Aided Design* CAD-11, 3 (1992) 341–352.
- L. T. Pillage, "Coping with RC(L) interconnect design headaches", Proc. IEEE/ACM Int. Conf. Computer-Aided Design, September 1995, pp. 246–253.
- L. T. Pillage, R. A. Rohrer, and C. Visweswariah, *Electronic Circuit and System Simulation Methods*, McGraw-Hill, Inc., 1994.
- 20. AS/X User's Guide, IBM Corporation, New York, 1996.
- W. Bowhill *et al.*, "Circuit implementation of a 300-MHz 64-bit second-generation CMOS alpha CPU", *Digital Technical J.* 7, 1 (1995) 100–118.
- E. G. Friedman, Clock Distribution Networks in VLSI Circuits and Systems, IEEE Press, New York, 1995.
- L. Sigal et al., "Circuit design techniques for the high-performance CMOS IBM S/390 parallel enterprise server G4 microprocessor", IBM J. Res. Development 41, 4/5 (1997) 489–503.
- H. B. Bakoglu, J. T. Walker, and J. D. Meindl, "A symmetric clock-distribution tree and optimized high speed interconnections for reduced clock skew in ULSI and WSI circuits", Proc. IEEE/ACM Int. Conf. Computer Design, October 1986, pp. 118–122.
- M. Nekili *et al.*, "Logic based H-trees for large VLSI processor arrays: A novel skew modeling and high-speed clocking method", *Proc. IEEE Int. Conf. Microelectronics*, December 1993, pp. 144–147.
- Y. Eo and W. R. Eisenstadt, "High-speed VLSI interconnect modeling based on Sparameter measurement", *IEEE Trans. Components, Hybrids, and Manufacturing Technology* CHMT-16, 5 (1993) 555–562.