# Hexagonal TSV Bundle Topology for 3-D ICs

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*Abstract*—Through-substrate vias (TSVs) are key for enabling 3-D integrated circuits (ICs). A hexagonal topology for TSV bundles in 3-D ICs is introduced in this brief. The topology exhibits superior symmetry as compared to the standard mesh topology. A comparison between the hexagonal and mesh topologies in terms of area per TSV, capacitive coupling, effective inductance, and shielding characteristics is offered. The hexagonal topology exhibits a reduction of 13% and 7% in, respectively, area per TSV and capacitive coupling. In addition, a two- to three-orders-ofmagnitude decrease in effective inductance within the hexagonal topology is observed.

*Index Terms*—Area per TSV, coupling capacitance, effective inductance, hexagonal topology, shielding, three-dimensional (3-D) integrated circuits (ICs), through-substrate vias (TSVs).

#### I. INTRODUCTION

**T** HROUGH-SUBSTRATE via (TSV)-based threedimensional (3-D) integrated circuits (ICs) are a field of increasing importance. 3-D integration is an exciting technology due to the smaller form factor, improved global signaling, and ability to integrate heterogeneous circuits within a single platform. The TSVs are short vertical interconnections (typically 20  $\mu$ m in length and 2 to 4  $\mu$ m in diameter [1], [2]) that carry a variety of signals (power, clock, and data) between different layers within a 3-D IC.

An important aspect of the 3-D IC design process is the placement of TSV bundles (multiple TSVs placed close to each other). These TSV bundles typically carry logically related multiple signals (*e.g.*, a multibit data bus [3]) or uniformly distributed power/ground lines between layers [4], [5]. Alternatively, a TSV bundle may be used to transfer a single signal surrounded by shielding TSVs. In this case, the primary signal could be a clock signal, a signal within a critical path, or a highly sensitive analog signal.

The pitch between two TSVs (minimum distance between the center of two adjacent TSVs) is predicted to be 4 to 8  $\mu$ m by the International Technology Roadmap for Semiconductors [2]. The standard structure of a basic TSV bundle is a threeby-three mesh topology [6], as shown in Fig. 1, where *p* is the pitch. This basic topology can be replicated for larger TSV

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Fig. 1. Three-by-three TSV bundle in a mesh topology. (a) Three-dimensional view, and (b) top view.



Fig. 2. Proposed hexagonal TSV bundle topology. (a) Three-dimensional view, and (b) top view. The distance between any two adjacent TSVs is the pitch p.

bundles (*e.g.*, five by five and seven by seven). The structure shown in Fig. 1(b), however, is not completely symmetric. While the distance from the TSV in the center to the four TSVs in the middle of the horizontal and vertical axes is p, the distance from the TSV in the center to the four TSVs on the two diagonal axes (the corner TSVs) is  $\sqrt{2}p$ . This structure is therefore asymmetric within the basic mesh TSV bundle. This structure is replicated in larger TSV bundles, making modeling and parasitic extraction of these TSV bundles challenging.

It is proposed here to replace the classical mesh topology for TSV bundles by a hexagonal topology, as shown in Fig. 2. The basic hexagonal TSV bundle is fully symmetric. This symmetry is maintained in larger TSV bundles. The hexagonal bundle has six edges, and the number of TSVs on each edge is n. An example of a basic hexagonal bundle with n = 1 is shown in Fig. 2(b) (see, for example, Fig. 8 for n = 2). The minimum pitch between any two adjacent TSVs within both the mesh and hexagonal topologies, shown in Figs. 1(b) and 2(b), is p. The number of TSVs within an n-by-n mesh bundle is  $n^2$ . The number of TSVs within a hexagonal bundle  $N_{\text{hexa}}$  with n TSVs on each edge is

$$N_{\text{hexa}} = 1 + 6 \cdot \sum_{i=1}^{n} (3i - 2).$$
 (1)

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Fig. 3. TSV sharing among basic adjacent bundles for (a) mesh, and (b) hexagonal topologies.

The characteristics of the hexagonal topology in terms of area, capacitive coupling, effective inductance, and shielding are discussed in this brief.

The rest of this brief is composed of the following sections. The area per TSV of the hexagonal topology is compared to the mesh topology in Section II. Capacitive coupling within the hexagonal TSV bundle is discussed in Section III. The effective inductance of hexagonal TSV bundles is discussed in Section IV. The shielding properties within hexagonal TSV bundles are provided in Section V. Some conclusions are offered in Section VI.

# II. AREA PER TSV

The area per TSV is the area of a bundle of TSVs divided by the effective number of TSVs ( $N_{\rm tsv}$ ) within that bundle. A TSV is considered completely within a bundle if the TSV is not shared with adjacent TSV bundles. Alternatively, if a TSV is shared among *n* adjacent basic bundles, the TSV area is effectively 1/n of a TSV for each of these bundles. This concept is illustrated for both mesh and hexagonal topologies in Fig. 3. In the mesh topology shown in Fig. 3(a), TSV V1 is shared among the basic bundles MB1 through MB4. In each of these bundles, V1 is treated as 1/4 of a TSV. Similarly, in the hexagonal topology, TSV V2 is shared among the bundles HB1, HB2, and HB3. V2 is therefore counted as 1/3 of a TSV for each of these bundles, as shown in Fig. 3(b).

By considering the basic bundles MB1 through MB4, shown in Fig. 3(a), the area and effective number of TSVs within a basic mesh bundle are, respectively,  $4p^2$  and 4. The effective number of TSVs in a basic mesh bundle is composed of one TSV (at the center of the bundle), four halves of a TSV (on the horizontal and vertical axes of the bundle), and four quarters of a TSV (at the corners of the bundle). By considering the basic bundles HB1, HB2, and HB3, shown in Fig. 3(b), the area and effective number of TSVs within a basic hexagonal bundle are, respectively,  $(3\sqrt{3}/2)p^2$  and 3. The effective number of TSVs in a basic hexagonal bundle is one TSV (at the center of the bundle) and  $(6 \cdot (1/3) =) 2$  TSVs (from the surrounding TSVs). The area per TSV of a mesh topology is therefore  $p^2$ , while the area per TSV of the hexagonal topology is  $(\sqrt{3}/2)p^2 \approx 0.87p^2$ . Hence, as listed in Table I, each TSV within a hexagonal topology requires 13% less area as compared to the mesh

TABLE I AREA CHARACTERIZATION OF MESH AND HEXAGONAL TOPOLOGIES OF TSV BUNDLES (*p* Is the Minimum Pitch Between Two Adjacent TSVs)

Parameter	Mesh topology	Hexagonal topology	Difference
Area of basic TSV bundle	$4p^2$	$\frac{3\sqrt{3}}{2}p^2$	35%
Effective number of TSVs	4	3	25%
Area per TSV	$p^2$	$\frac{\sqrt{3}}{2}p^2$	13.4%



Fig. 4. Hexagonal basic TSV bundle placed on a Manhattan grid.



Fig. 5. Capacitive coupling within basic TSV bundles for (a) mesh, and (b) hexagonal topologies.

topology. Alternatively, more TSVs can be included within a hexagonal TSV bundle.

Note that the hexagonal topology does not pose any additional manufacturing obstacles since all of the TSVs within a bundle are separated by technologically defined design rules. As described in [7], the etch area of each TSV is the same as in conventional contact lithography. The primary design rule for TSVs is the minimum pitch between any two TSVs. This requirement is satisfied within the hexagonal TSV bundles. Furthermore, the hexagonal topology is placed on a Manhattan grid, as illustrated in Fig. 4, similar to a mesh topology.

## III. CAPACITIVE COUPLING

Characterization of coupling capacitance enhances noise coupling analysis and parasitic extraction within 3-D ICs. An electrical model of the capacitive coupling with respect to a reference TSV for both the basic mesh and hexagonal TSV bundles is depicted in Fig. 5. The reference TSV  $T_{\rm ref}$  is the center TSV in each bundle topology, specifically TSV number 5 in the mesh topology and TSV number 7 in the hexagonal

topology. The coupling capacitance of a basic TSV bundle  $C_{\text{bundle}}$  is the total capacitive coupling from the surrounding TSVs within a bundle to the reference TSV. Two types of coupling capacitance (with respect to  $T_{\text{ref}}$ ) exist within a mesh bundle: 1) from the TSVs on the horizontal and vertical axes of the bundle, and 2) from the TSVs at the corners of the bundle. As depicted in Fig. 5(a), these capacitances are, respectively

$$C_{1,T_{\rm ref}} = C_{3,T_{\rm ref}} = C_{7,T_{\rm ref}} = C_{9,T_{\rm ref}} \triangleq C_{\rm diag}^{\rm mesh} \qquad (2)$$

$$C_{2,T_{\rm ref}} = C_{4,T_{\rm ref}} = C_{6,T_{\rm ref}} = C_{8,T_{\rm ref}} \triangleq C_{\rm orth}^{\rm mesh}.$$
 (3)

Due to the natural symmetry within the hexagonal bundle, the coupling capacitance (with respect to  $T_{\rm ref}$ ) is identical for all of the surrounding TSVs, as depicted in Fig. 5(b). The coupling capacitance to  $T_{\rm ref}$  from all of the surrounding TSVs for the basic hexagonal bundle is

$$C_{1,T_{\text{ref}}} = C_{2,T_{\text{ref}}} = C_{3,T_{\text{ref}}} = C_{4,T_{\text{ref}}}$$
$$= C_{5,T_{\text{ref}}} = C_{6,T_{\text{ref}}} \triangleq C^{\text{hexa}}.$$
 (4)

The coupling capacitance of the mesh and hexagonal topologies is, therefore, respectively

$$C_{\text{bundle}}^{\text{mesh}} = \sum_{i=1}^{8} C_{i,T_{\text{ref}}} = 4 \left( C_{\text{diag}}^{\text{mesh}} + C_{\text{orth}}^{\text{mesh}} \right)$$
(5)

$$C_{\text{bundle}}^{\text{hexa}} = \sum_{i=1}^{6} C_{i,T_{\text{ref}}} = 6 \cdot C^{\text{hexa}}.$$
(6)

The capacitive coupling between the TSVs is a strong function of the pitch between the TSVs. To compare the mesh and hexagonal bundle topologies in terms of capacitive coupling, a relationship in terms of the pitch is required. A closed-form expression for the coupling capacitance between two TSVs, previously described in [8], is approximated to characterize the coupling capacitance in terms of the pitch p between two TSVs

$$C_c = 7 \cdot 10^{-22} p^{-1.398}. \tag{7}$$

As depicted in Fig. 1(b),  $p_{\text{diag}} = \sqrt{2}p$ . Substituting this expression into (7) reveals the relationship between  $C_{\text{diag}}^{\text{mesh}}$  and  $C_{\text{orth}}^{\text{mesh}}$ 

$$C_{\text{diag}}^{\text{mesh}} = 7 \cdot 10^{-22} (p_{\text{diag}})^{-1.398}$$
  
=  $7 \cdot 10^{-22} (\sqrt{2}p)^{-1.398}$   
=  $(\sqrt{2})^{-1.398} 7 \cdot 10^{-22} p^{-1.398}$   
=  $0.616 \cdot C_{\text{orth}}^{\text{mesh}}$ . (8)

The coupling capacitance between any two TSVs with pitch p is the same regardless of the topology. Therefore,  $C_{\text{orth}}^{\text{mesh}} = C^{\text{hexa}}$ . Substituting (8) into (5) yields

$$C_{\text{bundle}}^{\text{mesh}} = 4 \left( 0.616 \cdot C_{\text{orth}}^{\text{mesh}} + C_{\text{orth}}^{\text{mesh}} \right)$$
$$= 6.464 \cdot C_{\text{orth}}^{\text{mesh}}$$
$$= 6.464 \cdot C^{\text{hexa}}. \tag{9}$$



Fig. 6. Coupling capacitance within the hexagonal TSV bundle normalized to the self-capacitance of the reference TSV.



Fig. 7. Coupling capacitance of the hexagonal and mesh TSV bundles evaluated using COMSOL [10].

Finally, from (6), a comparison between the coupling capacitance of the mesh and hexagonal bundles is

$$C_{\text{bundle}}^{\text{hexa}} = 0.93 \cdot C_{\text{bundle}}^{\text{mesh}}.$$
 (10)

The coupling capacitance of the hexagonal topology is therefore 7% smaller than the coupling capacitance of the standard mesh topology. Note that the TSV mesh bundle includes capacitive coupling from eight surrounding TSVs, while the hexagonal bundle includes capacitive coupling from only six TSVs. Although the number of surrounding TSVs in the mesh topology is greater, the comparison is accurate since capacitive coupling is a local phenomenon [1], [4]. The coupling capacitance within the hexagonal bundle normalized to the selfcapacitance of the reference TSV is extracted from the Ansys Q3D Extractor [9], as depicted in Fig. 6. Those TSVs placed farther from the center TSV within the hexagonal topology exhibit a negligible effect on the total capacitive coupling (with respect to the reference TSV).

To further validate this result, both the mesh and hexagonal bundles have been simulated using COMSOL [10], as depicted in Fig. 7. COMSOL is a finite element method simulator that solves Maxwell's equations. Both TSV bundle topologies have been evaluated for different pitches between TSVs. This evaluation confirms the advantage of lower coupling capacitance of the hexagonal bundle over a mesh bundle. The average



Fig. 8. Seven TSV bundles in hexagonal topology with uniformly distributed power/ground TSVs.

improvement in bundle capacitance of the hexagonal topology determined from COMSOL simulations is 11%, which closely corresponds to the analytic expression of (10).

## **IV. EFFECTIVE INDUCTANCE**

A hexagonal TSV topology with uniformly distributed power/ground TSVs [4] is depicted in Fig. 8. Unlike capacitive coupling, inductance is a long range phenomenon, requiring the identification of the current return path of each interconnect as well as the magnetic field lines of the adjacent current loops. The number of TSVs within a bundle also significantly affects the inductance as any additional TSV within a bundle provides an additional current return path. An accurate comparison of the mesh and hexagonal bundles should therefore include a similar number of TSVs. This requirement is challenging if symmetry within the bundles is maintained. Based on [1] and [11], the average mutual inductance  $L_{\rm mutual}^{\rm avg}$  is the total mutual inductance from all of the surrounding TSVs within the bundle to the reference TSV (excluding the self-inductance of  $T_{\rm ref}$ ) divided by the number of surrounding TSVs. The average mutual inductance is used here as a figure of merit to compare the different sizes and topologies of the two types of TSV bundles.

The total inductance of a TSV bundle for both a mesh and a hexagonal topology has been numerically evaluated by the Ansys Q3D Extractor. The mesh bundle is a five-by-five structure, whereas the hexagonal bundle has two TSVs on each edge (n = 2), as depicted in Fig. 8. Both bundles consist of uniformly distributed power and ground TSVs. The total number of TSVs in the mesh bundle is  $5^2 = 25$ . For the hexagonal bundle and from (1) for n = 2, the total number of TSVs is 31. These TSV bundles consist of TSVs with a radius of 1  $\mu$ m, length of 20  $\mu$ m, and copper material. A minimum pitch of 10  $\mu$ m is used for both bundle topologies. A comparison of the inductive properties between the mesh and hexagonal TSV bundle topologies is listed in Table II. The total and average mutual inductance of the hexagonal topology is approximately two to three orders of magnitude lower than the mesh topology. The reduction in mutual inductance is due to the symmetry of the hexagonal bundle. For each power TSV, there is a ground TSV. The power and ground TSVs carry current in opposite directions, effectively canceling the mutual inductance

TABLE II INDUCTANCE OF THE MESH AND HEXAGONAL TSV BUNDLES

Bundle topology	Number o in bui	of TSVs ndle	Total mutual inductance [pH]	Average mutual inductance [pH]
Mesh	9 25		-3.06 -3.65	-0.383 -0.152
Hexagonal	7 31		$-1.4 \cdot 10^{-3}$ 5.54 \cdot 10^{-2}	$-2.33 \cdot 10^{-4}$ $1.85 \cdot 10^{-3}$
		$\bigcirc$	ightarrow	ightarrow
Agg	ressor TSV	D	Victim TSV	•
		$\bigcirc$	0	$\bigcirc$

Fig. 9. Top view of shielding model for the mesh TSV bundle topology. D is the distance between the aggressor and victim TSVs.

with respect to the reference TSV [12]. This trait significantly reduces delay uncertainty caused by mutual inductance [13].

Note that both the total and average mutual inductance increases with larger TSV bundles for the hexagonal topology. This increase is due to a small inaccuracy in the placement of the TSVs within the hexagonal bundle. While a minimum pitch exists between any two adjacent TSVs, the horizontal distance between these TSVs is not a rational number  $((\sqrt{3}/2)p)$ . Higher accuracy may be used in the horizontal axis to reduce this error.

#### V. SHIELDING PROPERTIES

Shielding critical paths from high frequency aggressors using power and ground interconnect is an important design technique to reduce both delay uncertainty and short-circuit power [14], [15]. This technique can also be applied to TSVs passing critical data signals between different layers within a 3-D IC. A comparison of the hexagonal and mesh TSV bundles in terms of shielding a data signal in the center of a bundle is discussed in this section. The reference TSV (center of a TSV bundle) is considered the victim signal, while the aggressor TSV is placed at a distance D, ranging from 20 to 100  $\mu$ m from the victim, as depicted in Figs. 9 and 10, respectively, for the mesh and hexagonal TSV bundle topologies. A SPICE netlist, including all RLC parasitic impedances, is extracted from the Ansys Q3D Extractor and simulated using HSPICE [16]. The aggressor signal transitions from 0 to 1 V with a rise time of 100 ps. The peak noise is recorded at the victim TSV.

A comparison of the peak noise of both topologies is shown in Fig. 11. The victim TSVs within the mesh and hexagonal TSV bundles exhibit similar noise isolation, 1 to 3.1 mV for distances of 20 to 100  $\mu$ m. Note that within the hexagonal TSV bundle, only six TSVs are used as power/ground shielding.



Fig. 10. Top view of shielding model for the hexagonal TSV bundle topology. D is the distance between the aggressor and victim TSVs.



Fig. 11. Effect of distance from aggressor to victim TSV on peak noise for mesh and hexagonal TSV bundle topologies.

In the mesh topology, eight shielding TSVs are required. The hexagonal TSV bundle topology therefore exhibits similar or better noise isolation while requiring fewer TSVs than the mesh topology.

## VI. CONCLUSIONS

A hexagonal topology for TSV bundles in 3-D ICs is introduced in this brief. The hexagonal bundle exhibits natural symmetry as compared to the classical mesh topology. This symmetry is maintained across larger hexagonal bundles. The hexagonal topology requires 13% less area per TSV than the mesh topology. This advantage allows the integration of a larger number of TSVs within the same area. Capacitive and inductive coupling within TSV bundles for both the mesh and hexagonal topologies have also been compared. The hexagonal bundle exhibits 7% lower capacitive coupling and two to three orders of magnitude lower total and average mutual inductances as compared to the mesh topology. The shielding properties of the hexagonal topology have also been evaluated. The hexagonal topology exhibits similar or lower peak noise at the victim TSV while utilizing only six TSVs for shielding, whereas the mesh topology requires eight TSVs (utilizing  $\sim$ 50% more area).

Manufacturing hexagonal TSV bundles is similar to the mesh topology, guided by the etching area of conventional contact lithography. Each pair of TSVs within a hexagonal topology is separated by the minimum pitch; therefore, no additional manufacturing constraints are required. The hexagonal TSV bundle topology exhibits superior physical and electrical characteristics as compared to the mesh bundle topology.

#### REFERENCES

- V. F. Pavlidis and E. G. Friedman, *Three-Dimensional Integrated Circuit Design*. San Mateo, CA, USA: Morgan Kaufmann, 2009.
- [2] International Technology Roadmap for Semiconductors (ITRS), ITRS Technology Working Groups, 2011.
- [3] T. Sekiguchi, K. Ono, A. Kotabe, and Y. Yanagawa, "1-Tbyte/s 1-Gbit DRAM architecture using 3-D interconnect for high-throughput computing," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 828–837, Apr. 2011.
- [4] K. Xu and E. G. Friedman, "Scaling trends of power noise in 3-D ICs," VLSI J. Integr., vol. 51, pp. 139–148, Sep. 2015.
- [5] W. Yao, S. Pan, B. Achkir, J. Fan, and L. He, "Modeling and application of multi-port TSV networks in 3-D IC," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 32, no. 4, pp. 487–496, Apr. 2013.
- [6] R. Weerasekera, M. Grange, D. Pamunuwa, H. Tenhunen, and L. R. Zheng, "Compact modelling of through-silicon vias (TSVs) in threedimensional (3-D) integrated circuits," in *Proc. IEEE Int. Conf. 3D Syst. Integr.*, Sep. 2009, pp. 1–8.
- [7] M. Zervas, Y. Temiz, and Y. Leblebici, "Fabrication and characterization of wafer-level deep TSV arrays," in *Proc. IEEE Int. Electron. Compon. Technol. Conf.*, May 2012, pp. 1625–1630.
- [8] I. Savidis and E. G. Friedman, "Closed-form expressions of 3-D via resistance, inductance, and capacitance," *IEEE Trans. Electron. Devices*, vol. 56, no. 9, pp. 1873–1881, Sep. 2009.
- [9] Ansys Q3D Extractor. [Online]. Available: http://www.ansys.com/
- [10] COMSOL Multiphysics 4.3b, 2013. [Online]. Available: http://www. comsol.com/
- [11] A. E. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM J. Res. Develop.*, vol. 16, no. 5, pp. 470–481, Sep. 1972.
- [12] A. V. Mezhiba and E. G. Friedman, "Inductive properties of highperformance power distribution grids," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 6, pp. 762–776, Dec. 2002.
- [13] Y. I. Ismail and E. G. Friedman, *On-Chip Inductance in High Speed Integrated Circuits.* Boston, MA, USA: Kluwer, 2001, ch. 6.
- [14] E. Salman and E. G. Friedman, *High Performance Integrated Circuit Design*. New York, NY, USA: McGraw-Hill, 2012, ch. 6.
- [15] S. Kose, E. Salman, and E. G. Friedman, "Shielding methodologies in the presence of power/ground noise," *IEEE Trans. Very Large Scale Integr.* (VLSI) Syst., vol. 19, no. 8, pp. 1458–1468, Aug. 2011.
- [16] Synopsys HSPICE. [Online]. Available: https://www.synopsys.com/