Quasi-Adiabatic Clock Networks in 3-D Voltage Stacked Systems

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Abstract-Power delivery in three-dimensional (3-D) integrated systems poses several challenges such as high current densities, large voltage drops due to multiple levels of resistive vertical interconnect, and significant switching noise originating from transient currents within different layers. Voltage stacking is a power delivery technique that is highly compatible with 3-D integration due to the physical proximity between layers, enabling the efficient transfer of recycled current. Power noise in clock networks is, however, not inherently addressed by 3-D voltage stacking. In this brief, a quasi-adiabatic technique between multiple clock networks within 3-D voltage stacked systems is proposed. The technique exploits the proximity of the clock networks to enable mutual charging and discharging when the clock signals transition to the same voltage. During this transition, the clock distribution networks are isolated from the power grid, reducing simultaneous switching noise and current load. The maximum current is reduced by an additional 13% as compared to only voltage stacking, the maximum voltage noise is reduced by up to 72% when the clock networks are isolated from the power grids, and the clock networks pull nearly 50% less charge from the source. The proposed technique is evaluated on a 7 nm predictive technology model.

Index Terms—Three-dimensional (3-D) integration, charge sharing, clock network, power network, quasi-adiabatic, voltage stacking.

I. INTRODUCTION

■HREE-DIMENSIONAL integration is a platform for VLSI systems that offers benefits such as higher integration density, shorter interconnect, and heterogeneous systems [1]. Delivering power to a 3-D system requires special consideration due to the greater complexity posed by the multiple integrated layers [2], [3], [4]. Power and ground through silicon vias (TSVs) increase resistive and inductive noise present in 3-D power networks. Ensuring the integrity of the power system in those layers far from a voltage regulator is an important challenge as the vertical and horizontal impedances of the power network produce switching noise (both IR and Ldi/dt). Voltage stacking [5], [6], [7], [8] is an emerging power distribution strategy with a natural synergy with 3-D integration which mitigates many of the challenges in delivering power to a many-layered system. A voltage stacked system lessens the demands on the power delivery system by enabling sections of the system to recycle current. In 3-D voltage stacked systems, each layer is physically closed, enabling more efficient transfer of recycled current due to the short interconnect between layers.

In voltage stacked systems, the power rails require dedicated voltage regulators to manage current load imbalances [5], [6], [7]. These imbalances arise from the different switching activities between sections of a system. If the system is synchronized, and the impedance of the clock distribution networks is similar, these networks switch at the same time and draw similar currents. The networks can charge

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High voltage CLK_{hig} domain Low voltage CLK domain

Regulato

Fig. 1. Voltage stacked system with two voltage levels.

and discharge each other without dedicated regulators supplying additional current. The focus of this brief is on exploiting the physical proximity of clock distribution networks within a 3-D voltage stacked system to enable charge sharing. The proposed technique isolates the clock distribution network from the power grid during one of the two clock transitions, reducing power noise and current loads that degrade the power system.

This brief is organized as follows. An overview of voltage stacking and adiabatic systems is provided in Section II. The proposed approach of quasi-adiabatic charge sharing between 3-D clock networks in voltage stacked systems is described in Section III. Simulation results are presented in Section IV. Some conclusions are offered in Section V.

II. OVERVIEW OF VOLTAGE STACKING AND ADIABATIC SYSTEMS

Voltage stacking is a power delivery technique where current is recycled between sections of a system that operate at different voltages. These sections are called voltage domains. A high voltage is applied across the system, and the current used by a higher voltage domain is passed to the next lower voltage domain. A two-level voltage stacked system, where each domain has a clock input, is illustrated in Fig. 1. Rather than connecting two domains in parallel, the two domains are connected in series. The current sourced by the higher voltage domain is passed to the lower voltage domain. Each domain has a different current load; dedicated voltage regulators supply additional current when the recycled current cannot satisfy the current needs of the lower voltage domain (assuming the voltage domains are serially placed in ascending current requirements). These regulators are illustrated in Fig. 1. Voltage stacking reduces the deleterious effects of high current on the power distribution network [5], [6], [9]. The reduced current densities that result from the serially connected voltage domains also lower the likelihood of hillock and void defects within the power grid caused by electromigration [10]. The dedicated regulators for each voltage domain mitigate IR drops within the power distribution networks and reduce simultaneous switching noise by isolating the power grids of each domain [9], [11], [12].

An adiabatic process is a thermodynamic process where no heat exchange occurs [13], [14], [15], [16]. In the context of adiabatic CMOS logic, the voltage difference between the drain and source for every device not operating in the cutoff region is kept as low as

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Fig. 2. Circuit topology for proposed quasi-adiabatic technique. During φ_1 , CLK_{HIGH} and CLK_{LOW} transition to the same voltage level. During φ_2 , CLK_{HIGH} transitions to $V_{DD,high}$, and CLK_{LOW} transitions to GND.

possible. The current that passes through each transistor is therefore small, drastically reducing the system-wide power consumption. As the transistor returns to the cutoff region, the current used to charge the load capacitance is recovered and can be reused to charge another load capacitance. Adiabatic systems, therefore, require a supply voltage that periodically switches between 0 V and $V_{\rm DD}$, which allows the voltage across the transistors to gradually change. This approach negates the fast switching required in high-speed circuits and introduces additional challenges to power delivery such as slew rate concerns.

Quasi-adiabatic techniques have also been proposed [17], [18], [19], [20] to balance the power savings of adiabatic systems with the higher speed of traditional circuits. One such technique uses a support capacitor. The charge on the load capacitances is stored on the support capacitor and reused during the following clock cycle [20]. This technique is considered quasi-adiabatic since the technique lacks a switching supply voltage, operates at high speeds, and does not recycle all of the charge. As described in the next section, the technique proposed herein combines the proximity of the different voltage domains enabled by 3-D integration with quasi-adiabatic charge sharing between the load capacitances.

III. QUASI-ADIABATIC 3-D CLOCK DISTRIBUTION NETWORKS

The proposed quasi-adiabatic technique between clock distribution networks is described in this section. While quasi-adiabatic techniques typically reduce energy consumption, the objective of this approach is to reduce simultaneous switching noise and current load within a voltage stacked system. To achieve this objective, the clock networks between adjacent voltage domains mutually charge and discharge without pulling current from the power grid, recycling charge in a quasi-adiabatic fashion. The clock signals are inverted to ensure that both signals transition to the same voltage. Two clock signals on separate layers are illustrated in Fig. 2. CLK_{LOW} is the clock signal for the low voltage domain (GND to $V_{DD,low}$), and CLK_{HIGH} is the clock signal for the high voltage domain ($V_{DD,low}$ to $V_{\text{DD,high}}$). φ_1 is the clock phase during which CLK_{LOW} undergoes a low-to-high transition, and φ_2 is the clock phase when CLK_{LOW} undergoes a high-to-low transition. During φ_1 , CLK_{LOW} and CLK_{HIGH} are connected to mutually charge and discharge. During this phase, the clock networks are isolated from the power network. To reliably pass the shared current without breaking down the transistors due to the high voltage difference, two transistors are serially connected to the clock networks. One transistor is for the higher voltage range, and the other transistor is for the lower voltage range. These devices



Fig. 3. Clock buffer for quasi-adiabatic clocking scheme. Note that CLK_{HIGH} and CLK_{LOW} are opposite phase, i.e., inverted.

are depicted in Fig. 2 as shared pass transistors, since these devices enable quasi-adiabatic recycling of charge. During φ_2 , the shared pass transistors are turned off; CLK_{LOW} is connected to the lower voltage (GND), and CLK_{HIGH} is connected to the higher voltage ($V_{DD,high}$).

The pull-up, pull-down, and shared pass transistors are placed within an intermediate (or interposer) layer between the high-voltage layer and the low-voltage layer. This approach is adopted to ensure that the impedances of the clock networks are symmetric. Placing the switches within the intermediate layer ensures that a TSV exists in both clock networks. The resulting symmetry mitigates the degradation of the clock signals. This approach also allows both clock signals to be synchronized by a global clock signal sourced from the intermediate layer.

The circuit shown in Fig. 3 realizes the switches depicted in Fig. 2. The input clock signal CLK_{IN} functions as the global clock signal. In this case, CLK_{IN} is in the lower voltage domain. The clock buffer produces signal S_{low} which controls transistors M1 and M2. The stacked voltage level shifter produces signal S_{high} which controls transistors M3 and M4. The level shifter uses the Tong topology [21] and introduces a 20 ps delay. Note that M2 and M3 are shared pass transistors, as illustrated in Fig. 2. This circuit topology drives both clock distribution networks, ensuring that the clock signals are synchronized and share charge during φ_1 . The clock distribution networks are effectively isolated from the power grid, reducing both the maximum current load and power noise.

IV. PERFORMANCE AND NOISE CHARACTERISTICS OF QUASI-ADIABATIC 3-D CLOCK DISTRIBUTION NETWORKS

The performance and noise characteristics of the proposed quasi-adiabatic clocking approach are described in this section. As previously discussed, voltage stacked systems typically use a dedicated voltage regulator for each voltage domain to manage current load imbalances. To compare the proposed approach with other clocking schemes, the clock driver incorporates an intermediate voltage. Note that this circuit topology can produce both same-phase clocking and opposite-phase clocking. Without V_{DD,low}, only opposite-phase clocking is produced, as illustrated in Fig. 4(b). The following clocking schemes are considered: 1) unstacked scheme-the clock signals have the same phase and voltage range; 2) same-phase scheme-this voltage stacked scheme features a regulated $V_{DD,low}$ between the high voltage clock signal and the low voltage clock signal; 3) oppositephase scheme-this scheme only differs from same-phase clocking in that the clock signals have opposite phase; and 4) proposed scheme-opposite-phase clocking without a regulated voltage to enable quasi-adiabatic recycling of charge between clock networks.

The energy, maximum current, charge from the voltage source, and average power noise of each clocking approach are listed in Table I;



Fig. 4. Voltage stacked clock driver. (a) With an intermediate voltage regulator. This clock driver topology enables same-phase clocking and opposite-phase clocking. (b) Clock driver without an intermediate voltage regulator. This clock driver topology only enables opposite-phase clocking.

TABLE I Comparison of Energy, Maximum Current, Charge From Source, and Average Power Noise of Each Clocking Scheme

| Clocking | Total | Maximum | Charge | Average power | |
|----------------|--------|---------|-------------|---------------|-------------|
| scheme | Energy | current | from | noise (mV) | |
| | (pJ) | (mA) | source (pC) | φ_1 | φ_2 |
| Unstacked | 1.62 | 2.90 | 3.25 | 3.8 | 5.1 |
| Same phase | 1.67 | 1.94 | 3.25 | 1.9 | 2.8 |
| Opposite phase | 1.64 | 1.57 | 1.78 | 0.5 | 2.8 |
| Proposed | 1.63 | 1.57 | 1.64 | 0.2 | 2.9 |

33% less current due to voltage stacking is required with the same-phase scheme as compared to the unstacked scheme. Moreover, the opposite phase and proposed schemes require approximately 46% less current. The total energy consumption per period is approximately the same for each clocking scheme. This similar energy in each scheme is due to the transistors passing similar currents. The difference is due to the current in the unstacked scheme being entirely sourced by the power grid, while the current is sourced from different parts of the system in the other schemes. The total energy of the unstacked scheme is slightly less since this scheme lacks a level shifter. The charge supplied by the source is the integral of the current passing through each power rail during one clock period. The proposed scheme requires nearly half of the charge as the unstacked or same-phase schemes. This behavior reduces the charge pulled from the source due to the charge recycling that occurs during φ_1 . The opposite-phase scheme pulls comparable charge from the source as the proposed scheme, but some charge is sourced by $V_{DD,low}$ to maintain a constant voltage. Note that this effect only represents the charge pulled by the clock networks, not the entire system. The average power noise is listed in Table I in two separate columns; the first column describes when CLK_{LOW} transitions high (φ_1), and the second column describes when CLK_{LOW} transitions low (φ_2). Note that the average noise voltage is relatively low since the average is over half the clock period (2.5 ns). The circuit analysis is validated assuming a 7 nm predictive technology model [22]. A clock period of 5 ns is assumed. The peak power noise is discussed later in this section. The proposed scheme exhibits the lowest average noise during φ_1 . Low noise is expected during this phase since the clock networks are isolated from the power grid. The noise of the proposed scheme is slightly higher during φ_2 as compared to the same-phase



Fig. 5. Peak noise voltage per power rail for each clocking scheme.



Fig. 6. Maximum voltage drop between each power rail scheme: GND, $V_{\text{DD,low}}$, and $V_{\text{DD,ligh}}$ during (a) φ_2 and (b) φ_2 .

and opposite-phase schemes but lower than the unstacked scheme. The average power consumption of the level shifter is 19.3 μ W.

The benefits of the proposed approach are highlighted when considering the peak power noise. The peak noise of each power rail (GND, $V_{DD,low}$, and $V_{DD,high}$) is shown in Fig. 5 for each clocking scheme. Note that this figure illustrates the peak noise produced during φ_1 , the clock phase when CLK_{LOW} undergoes a low-to-high transition. For the same-phase scheme, power rails $V_{\text{DD,low}}$ and $V_{\text{DD,high}}$ experience significant noise during this phase. The opposite-phase scheme experiences high noise on the intermediate power rail due to a small synchronization offset between CLK_{LOW} and CLK_{HIGH} , causing the regulator to supply current to both clock networks. The proposed scheme reduces noise from all of the power rails by isolating the clock networks from the power rails. The noise voltage for the proposed scheme primarily originates from the voltage level shifter used for synchronization. Note that the unstacked scheme does not include a $V_{\text{DD,high}}$ power rail.

The proposed scheme is also independent of the inductance of the power rails. This characteristic is significant considering the complexity of inductance extraction of power grids in 3-D VLSI systems [1], [23], [24], [25]. The peak voltage drop of all three power rails with increasing power grid inductance is depicted in Fig. 6. The peak noise voltage for φ_1 is shown in Fig. 6(a), while the peak noise voltage for φ_2 is shown in Fig. 6(b). For φ_1 , the peak noise voltage is considerably lower for the proposed clocking scheme and remains low with increasing power grid inductance. The peak noise voltage of the other two voltage stacked clocking schemes increases in proportion to the increase in inductance. The peak noise voltage of the proposed scheme is, however, slightly higher (except as compared to the unstacked scheme) when the clock networks transition to opposite voltages. This behavior is caused by the unregulated node between M2 and M3. During the transition, the effective difference in voltage between the ground and the unregulated node is slightly larger

TABLE II TRANSITION TIME OF EACH CLOCKING SCHEME

| Clocking Scheme | Low-to-high transition (ps) | | High-to-low transition (ps) | |
|--------------------|--------------------------------|---------------------|--------------------------------|---------------------|
| | CLKLOW | CLK _{HIGH} | CLK _{LOW} | CLK _{HIGH} |
| Unstacked | 678 | 678 | 576 | 576 |
| Same phase | 669 | 667 | 563 | 566 |
| Opposite phase | 653 | 667 | 566 | 556 |
| Proposed | 605 | 665 | 566 | 605 |

than the regulated case. This effect causes a larger current to flow to ground, resulting in a higher noise spike. While this behavior produces more noise during the second phase, the relatively quiet phase can be exploited by latching data during φ_1 . This approach ensures that when most data paths switch, the noise produced by the data latches does not add to the noise generated by the clock networks.

The transition times of the clock signals for each clocking scheme are listed in Table II. In the stacked schemes, CLK_{HIGH} exhibits a slightly faster low-to-high transition, and CLK_{LOW} exhibits a slightly faster high-to-low transition due to the shared pass transistors supplying some additional charge. In the proposed scheme, both signals exhibit the same transition time when CLK_{LOW} transitions high and CLK_{HIGH} transitions low. This behavior is expected during the transition in which the two clock networks charge and discharge each other. This transition time is the average of the unstacked lowto-high and high-to-low transition times. The opposite-phase scheme does not exhibit the same behavior since the regulated node restricts the current passing through the shared pass transistors.

Since the clock drivers are placed within the intermediate layer, the high and low voltage layers, shown in Fig. 2, save the area that would typically be used for the clock drivers. This approach also reduces the complexity of the power delivery system in the high and low-voltage layers since delivering power to the clock drivers is performed exclusively within the intermediate layer.

V. CONCLUSION

A clocking technique tailored for 3-D systems that combines voltage stacking with quasi-adiabatic techniques is described here. The technique isolates the clock networks of a 3-D voltage stacked system from the power networks when two clock signals from separate voltage domains transition to the same voltage. The technique simultaneously synchronizes and isolates the clock networks from the power grid by placing shared transistors between the clock networks that enable mutual charging and discharging. The proposed technique reduces the maximum current load by 45% and reduces the charge pulled from the source by nearly 50%.

The proposed technique produces a relatively constant, low noise voltage with increasing inductance when the shared pass transistors are on, while the other clocking schemes increase the noise voltage in proportion to the inductance. Slightly higher noise is produced when the clock signals transition to separate voltages; however, the total simultaneous switching noise caused by the clock networks and data latches is lower if the data are latched when the shared pass transistors are on. The transition times of the clock signals are also positively impacted by the proposed technique. The transition time during φ_1 is the same for each clock signal. Future work includes the development of a methodology to ensure that those clock networks sharing charge are symmetric and tolerant to process variations. The frequency limitations and skew tolerance of the technique will also be explored. A clock buffer circuit that allows the clock signals to operate at a fraction of the frequency will be developed. Methods to reduce noise when the shared pass transistors are off will also be explored.

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