

Injection-Locked Clocking: A New GHz Clock Distribution Scheme

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Abstract— We propose a new GHz clock distribution scheme, injection-locked clocking (ILC). This new scheme uses injection-locked oscillators as the local clock regenerators. It can achieve better power efficiency and jitter performance than conventional buffered trees with the additional benefit of built-in deskewing. A test chip is implemented in a standard 0.18 μ m digital CMOS technology. It has four divide-by-2 ILOs at the leaves of a 3-section H-tree, generating 5GHz local clocks from the 10GHz input clock with 17% locking range and no phase noise degradation. Measured jitter of generated clocks is lower than that of the input signal. Two local clocks can be differentially deskewed up to 80ps relative to each other. The test chip consumes only 7.3mW excluding test-port buffers.

I. INTRODUCTION

Clock distribution will increasingly be one of the most challenging tasks in microprocessors and other high-speed VLSIs. The 2005 ITRS roadmap projects that the on-chip clock speed will continue to rise to over 10 GHz as early as 2008, and over 20 GHz by 2012 [1]. Even though the device feature size will shrink, the chip size will remain constant (about 16.7 mm from edge to edge [1]) as more functions are added. If current clocking schemes continue to be used, it is expected that skew and jitter will consume an increasingly large portion of each clock cycle, and hence the time available for critical path will eventually be less than the technology-allowed minimum delay beyond the 32nm node in 2013. This will largely defeat the purpose of any further clock speed increase. In the meantime, the power consumption in clock distribution networks has also become a serious problem. Currently, about 40% of total power consumption of a high-performance microprocessor is used by the clocking circuitry [2]. As both clock speed and transistor count increase, the projected power consumption of a high-performance microprocessor will exceed the power density limit set by packaging [1]. Therefore, we need a new clocking solution that can achieve better skew and jitter performance while consuming less power.

Optical interconnect potentially offers smaller delays and lower power consumption than electrical ones, and is promising for the global clock distribution network [3]. However, there are still great challenges in its silicon implementation, particularly for on-chip electrical-optical modulators [4]. Among the proposed electrical solutions, a family of synchronized clocking techniques, such as distributed clocking [5], rotary clocking [6], and resonant clocking [7], [8], have recently been demonstrated to lower power consumption of clocking distribution. They are essentially synchronized, distributed, coupled oscillator arrays, and thus have the problems of phase uncertainty and synchronization difficulty [9]. They also add new constraints to the design of the global clock-distribution tree since the latter becomes part of the resonator for the

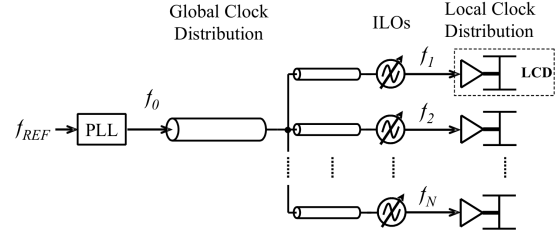


Fig. 1. Injection-locked clocking.

oscillator array. Further, these synchronized clock schemes are generally incompatible with design-for-testability (DFT) since all (local) clock signals are coupled and hence difficult to be independently controlled in testing. Therefore, it is highly desirable to explore new solutions that are compatible with existing IC infrastructures as well as current design and testing methodologies.

In this paper, we propose a new clock distribution scheme which utilizes injection-locked oscillators as the local clock generators. The new scheme has better jitter performance, consumes less power, and provides built-in deskew capability. We will introduce the proposed scheme in Section II, and then demonstrate it with the implementation (Section III) and measurement results (Section IV) of a chip prototype.

II. INJECTION-LOCKED CLOCKING

Figure 1 shows the proposed new clocking scheme. We use injection-locked oscillators (ILOs) to generate local clocks, which are synchronized to the global clock through injection locking [10], [11]. Note that this is different from resonant clocking [8], where all the oscillators are coupled together. Further, ILOs can be constructed as frequency multipliers [12] or dividers [13], [14], and hence this scheme enables local clock domains at higher ($n \times f_0$) or lower speed (f_0/m) than the global clock (f_0). Such a global-local clocking scheme with multiple-speed local clocks offers significant improvements over conventional single-speed clocking scheme in terms of power consumption, skew, and jitter.

A. Power Efficiency

The combination of a low-speed global clock and high-speed local clocks can reduce the power consumption in the global clock distribution network. The conventional approach, however, would require multiple power-hungry phase-locked loops (PLL) for frequency multiplication. An ILO consumes much less power than a PLL because of their circuit simplicity [15].

Running at the same clock speed, injection-locked clocking can also significantly reduce the power consumption in the

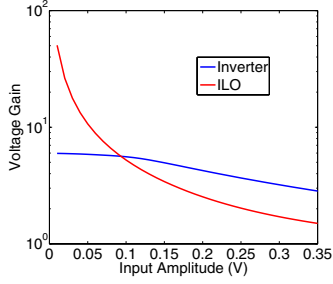


Fig. 2. Voltage gain of an inverter and an injection-locked oscillator at different input signal levels.

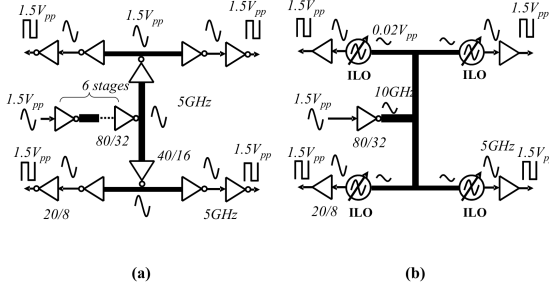


Fig. 3. Clock signals in (a) a traditional buffered H-tree and (b) injection-locked clocking. Buffer sizes are shown in the figures as Wp/Wn with gate length of $0.18\mu m$.

global clock distribution network compared to conventional clocking. As a synchronized oscillator, an ILO effectively has very large voltage gain when the injection signal amplitude is small, while the gain of an inverter is much smaller (Fig. 2). In other words, ILOs have higher sensitivity than buffering inverters. Therefore, the clock signal amplitude can be much smaller in the new clocking scheme, which means less power loss on the global-clock distribution interconnects. The number of clock buffers can also be reduced, which lowers the power consumption further.

For example, a conventional buffered H-tree is constructed using transmission lines that are identical to those in the test chip (see Section III), and the buffer sizes are optimally designed (Fig. 3-a). Simulation shows that it consumes 39mW to distribute 5GHz clock signals with 1.5V rail-to-rail voltage swing. In comparison, an injection-locked clocking tree is also constructed using the core identical to that of the test chip, but drives the same load as the buffered tree (Fig. 3-b). The global clock signal amplitude is reduced to 0.01V, and the number of buffers needed to drive the H-tree is reduced from 6 to 1. Hence it only consumes 13.5mW. Note that this comparison actually favors the buffered tree since divide-by-2 ILOs are used in the injection-locked tree, with its global clock at 10GHz. If non-dividing ILOs are used, the power consumption of the injection-locked tree will be even lower.

B. Skew Reduction and Deskew Capability

Because the number of buffers is reduced in the new clocking scheme, one of the major sources of skew, clock buffer mismatch, is also reduced compared to conventional

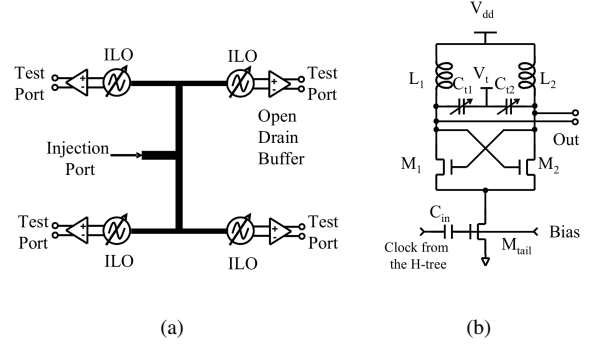


Fig. 4. Schematic of (a) the test chip and (b) a divide-by-2 ILO used.

clocking. In addition, the new scheme provides a possible method for deskewing local clocks. Similar to the phase error in a PLL, the phase difference between the input and output signals of an ILO is a function of their frequency difference. When the center frequency of an ILO is tuned, therefore, the phase of the output signal will shift accordingly. The phase shift is a monotonic function of the frequency shift, and the function is quite linear within the locking range [16]. This phase tunability enables ILOs to also serve as built-in “deskew buffers”. In turn, removing dedicated deskew buffers not only saves power, but also reduces their vulnerability to power supply noise.

C. Jitter Suppression

Reduced number of clock buffers also means less pick-up of power supply and substrate noise and hence less jitter generation and accumulation. In addition, similar to a PLL, the ILO shows a high-pass filtering for the phase noise due to the internal noise sources. Because of the large “loop bandwidth” of an ILO, the internal phase noise of the oscillator is largely suppressed, and has little effect on the ILO jitter [15]. For jitter transfer, phase noise from the input signal at large offset frequency is attenuated because of the low-pass noise transfer function similar to a PLL. Because short-term (cycle-to-cycle) jitter matters in clocking, which is largely determined by the phase noise at large offset frequency [17], an ILO can potentially suppress the input signal jitter. Overall, injection-locked clocking is likely to achieve better jitter performance than conventional clocking.

III. TEST CHIP IMPLEMENTATION

A test chip is designed and implemented in a standard $0.18\mu m$ digital CMOS technology with low-resistivity substrate (Fig. 4(a)). A 3-section H-tree mimics the global clock distribution network in real microprocessors. The root of the H-tree is directly connected to a ground-signal-ground (GSG) pad to facilitate testing (Fig. 5). The leaves of the H-tree are four divide-by-2 ILOs, which divide the input 10GHz clock signal into 5GHz local clocks. The differential outputs of ILOs then drive four open-drain differential amplifiers, which are directly connected to output RF pads.

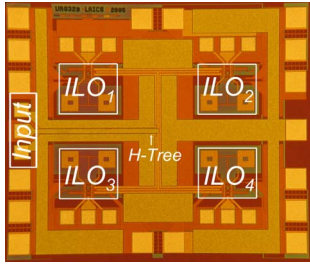


Fig. 5. Chip micrograph of the test chip. The whole chip size is $1.5\text{mm} \times 1.3\text{mm}$, and each ILO occupies $0.25\text{mm} \times 0.22\text{mm}$. The H-tree sections measure $500\mu\text{m}$, $280\mu\text{m}$, and $290\mu\text{m}$, respectively, from root to leaves.

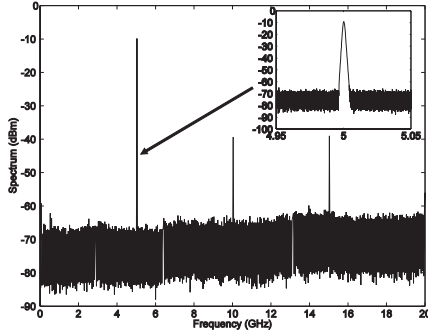


Fig. 6. Spectrum of the generated local clock signal from ILO1, identical to that from other ILOs on-chip.

The differential divide-by-2 ILO [13] is shown in (Fig. 4(b)). This is essentially a differential LC oscillator, with the input signal injected into the gate of the tail transistor. We chose this ILO for the test chip because of its well-understood operation and good performance. Spiral inductors are made on metal 5 with a quality factor about 4 at 5GHz. Such low Q is not a problem for ILO operation and actually helps increase the locking range. If better metal is available, the power efficiency can be further improved. NMOS transistors biased in inversion region are used as varactors to tune the ILO center frequency, which in turn changes the phase of the local clocks for deskewing purpose.

The H-tree is constructed using coplanar-waveguide (CPW) transmission lines. Bottom shield is used to reduce substrate coupling in a real microprocessor environment. This limits the maximum characteristic impedance of the transmission line to be just over 40Ω in this technology. So the transmission lines from the H-tree leaves to the root are designed to be 40Ω , 20Ω and 10Ω , respectively, in order to achieve impedance matching at all junctions. Width of signal and ground lines, spacing between them, and choice of metal layers are also optimized for minimizing the clock propagation loss.

IV. MEASUREMENT RESULTS

The test chip is measured using an RF probe station. The input is a sinusoidal signal from a continuous-wave (CW) signal generator. The power supply voltage is 1.4V. The spectra of the local clock signals generated by the four ILOs are almost identical, and one of them is shown in Fig. 6.

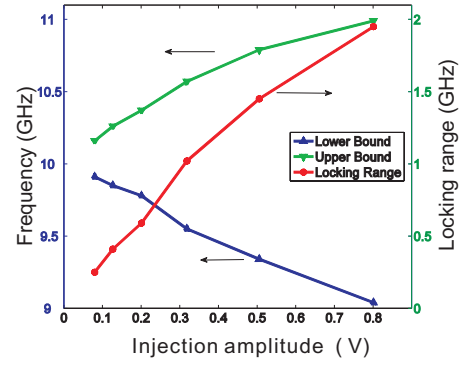


Fig. 7. Locking range of ILO1, identical to that of other ILOs on-chip.

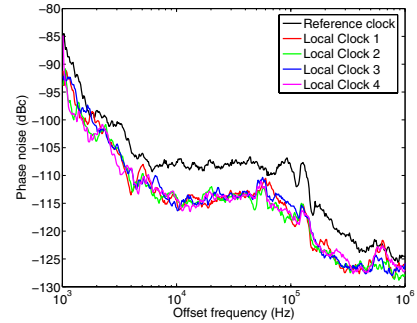


Fig. 8. Phase noise of reference clock and 4 output clocks at different positions on chip.

The locking range of ILOs on the test chip is found to be identical, and that of ILO1 is shown in Fig. 7. The injection signal amplitude is calculated from the measured incident power and reflection coefficient (S11) at the root of the H-tree. It can be seen that when the input signal has rail-to-rail swing (1.4V), the locking range is about 17%, which is sufficient for both accommodating process/temperature variation and deskew tuning (see below).

Phase noise of both the input and output clock signals are shown in Fig. 8. The 6dB reduction (up to about 500kHz offset) because of the divide-by-2 operation is evident, which

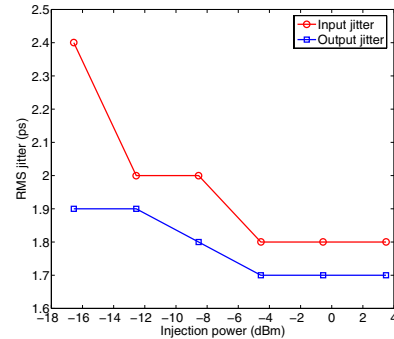
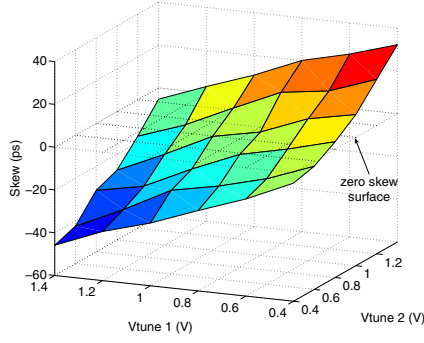
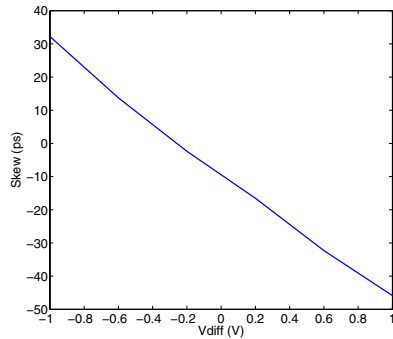


Fig. 9. Jitter characteristics.



(a)



(b)

Fig. 10. Deskew capability of ILC. (a) deskewing when tuning ILO1 and/or ILO2; (b) deskewing when tuning ILO1 and ILO2 differentially. The skew is measured between the two output clock signals of ILO1 and ILO2. Note that there is some imbalance between ILO1 and ILO2 caused by mismatch in the clock distribution tree and measurement system.

shows that the internal ILO noise is suppressed by injection locking. Fig. 9 shows the long-term RMS jitter of both the input and output signals measured using a self-referenced jitter measurement method with a sampling oscilloscope [17]. The output timing jitter is even less than that of the input signal. Considering the frequency division, this result clearly demonstrates that ILOs can serve as a PLL and clean up the clock signal.

The deskew capability of injection-locked clocking is demonstrated in Fig. 10. Fig. 10(a) shows the whole deskew surface when tuning ILO1 by V_{tune1} , and/or ILO2 by V_{tune2} . One particular tuning example is shown in Fig. 10(b), where V_{tune1} and V_{tune2} are tuned differentially, and the deskew range is up to 80ps. Because of the large deskew range, small imbalance in the global clock tree can be easily compensated, which greatly relaxes the requirement on the design and layout of the clock distribution network.

The test chip consumes a total power of 52.8mW, where 45.3mW comes from the 1.8V-supplied open-drain buffers. The ILOs core circuitry working under 1.4V Vdd only con-

sumes 7.3mW when biased low and injection signal is 6dBm. The bias circuitry consumes 0.2mW.

V. CONCLUSION

The proposed injection-locked clocking can significantly improve the power efficiency and jitter performance of a GHz clock distribution network. The built-in deskewing capability further reduces the system complexity and power consumption. The benefits will be even greater when this new clocking scheme is applied to future multi-core microprocessors and other high performance system-on-a-chip (SoC) systems because it maintains synchrony between communicating processors.

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