Nanospintronics Based on Magnetologic Gates

Hanan Dery, *Member, IEEE*, Hui Wu, *Member, IEEE*, Berkehan Ciftcioglu, *Member, IEEE*, Michael Huang, *Member, IEEE*, Yang Song, Roland Kawakami, Jing Shi, Ilya Krivorotov, *Member, IEEE*, Igor Žutić, and Lu J. Sham

***Abstract*—We present a seamless integration of spin-based memory and logic circuits. The building blocks are magnetologic gates based on a hybrid graphene/ferromagnet material system. We use network search engines as a technology demonstration vehicle and simulate a high-speed, small-area, and low-power spin-based circuit.**

***Index Terms*—Network search engines, spintronics.**

THE CONTINUED Moore's law scaling in CMOS integrated circuits poses increasing challenges to provide low-energy consumption, sufficient processor speed, bandwidth of interconnects, and memory storage [1]. Currently, microprocessors rely on the von Neumann architecture consisting of central processing units connected by some communication channel to memory. The bottleneck due to the communication access and memory access is the underlying reason for the widening gap between the fast improving transistor performance and our relatively stagnant programs execution speed. Such bottlenecks are particularly obvious for data-intensive applications, where most of the actions involve accessing or checking data (rather than doing complex computation). Network routers are a classical example where the Internet Protocol address is compared with a list of patterns to find a match. Conventional CMOS implementation of such circuits suffers from scalability issues, making them ineffective for larger search problems that are increasingly important to modern workloads. In this brief, we propose a paradigm change for these applications using spintronics [2]–[5]. We design a 3.2-Mbit spintronic search engine with a < 1 mm^2 total chip area and 23-W power consumption.

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H. Dery, H. Wu, B. Ciftcioglu, and M. Huang are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: hanan.dery@rochester.edu).

Y. Song is with the Department of Physics, University of Rochester, Rochester, NY 14627 USA.

R. Kawakami and J. Shi are with the Department of Physics, University of California Riverside, Riverside, CA 92521 USA.

I. Krivorotov is with the Department of Physics, University of California Irvine, Irvine, CA 92697 USA.

I. Žutić is with the Department of Physics, State University of New York at Buffalo, Buffalo, NY 14260.

L. J. Sham is with the Department of Physics, University of California San Diego, La Jolla, CA 92093 USA.

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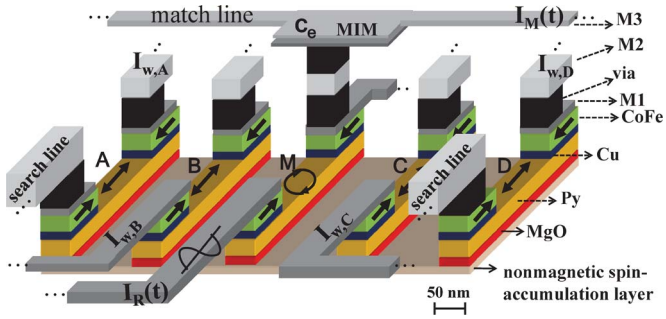

Fig. 1. MLG in a search engine matrix. Spin accumulation in the nonmagnetic layer is governed by the magnetic directions of the A–B and C–D contacts pairs. This accumulation determines the logic result. Using STT, the logic operands are encoded via individual writing currents across the low resistive and all-metallic path (CoFe/Cu/Py/Cu/CoFe). $I_{W,A}$ and $I_{W,D}$ encode the search bits. $I_{W,B}$ and $I_{W,C}$ encode the key bit. Readout is triggered by the current signal $I_R(t)$ that perturbs the magnetization of the middle contact. The logic output is the resulting transient current $I_M(t)$ across the metal–insulator–metal capacitor C_e. A search or a reading current activates, respectively, all of the MLGs along its search or match line. A metallic via and interconnect layers (M1–M3) are embedded in an oxide (not shown for clarity).

It consists of 25 000 words of 128 bits. The performance is assessed via circuit simulation.

A Magnetologic gate (MLG) is adopted as a basic building block due to its favorable properties of spin amplification, speed, and scalability [2]. Here, we summarize the MLG operation. Detailed explanations are provided in [2] and [6]. Fig. 1 shows a universal and reconfigurable MLG that consists of five ferromagnetic (FM) electrodes on top of a nonmagnetic layer. FM regions are inherently nonvolatile, preserving the direction of magnetization without power supply. This nonvolatility has been extensively used for robust information storage in magnetic hard drives and magnetic random access memory (MRAM) devices [7]. Here, we show how it can also be used for high-performance magnetologic. The magnetization itself reflects that the FM electrode has an unequal number of electrons with two different spin projections (up and down; minority and majority). The MLG design employs a stack of FM layers where the elongated permalloy layer (Py) is the free magnetic layer into which the information is encoded. The MLG operation relies on the generation of nonequilibrium spin accumulation when spin-polarized electrons tunnel from the free layer into the nonmagnetic layer via the MgO tunneling barrier. The magnitude of the spin accumulation in the nonmagnetic layer strongly depends on the relative orientation of the magnetization directions in the free layers of the MLG [8], [9]. Of the five FM contacts, the middle contact (M) is used for readout, and the remaining contacts (A, B, C and D) are logic operands whose values are defined by the magnetization

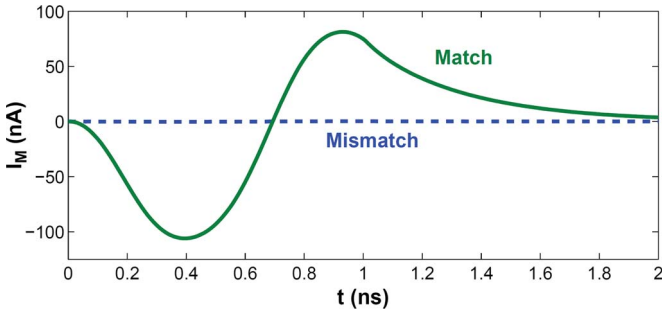

Fig. 2. Modeled transient current response across the middle contact of a graphene-based MLG set for matching between the stored (B and C) and search (A and D) bits. The response is to a 1-ns in-plane rotation of the magnetization direction of M. The bias is $V_{dd} = 1$ V, and the external capacitor is $C_e = 1$ fF. The five contacts are 50-nm wide and 100-nm deep in the z-direction (see Fig. 1). The spacing between contacts is 30 nm. The resistance and intrinsic capacitance of each contact are, respectively, 200 kΩ and 0.4 fF.

direction. The output state is given by the Boolean expression {(A XOR B) OR (C XOR D)}. Programming B and C results in a universal set of four logic operations between A and D.

The logic operation is triggered by perturbing the magnetization direction of M. The electrical response is governed by the potential level in the middle contact. In the steady state, the potential level is set by the zero electrical current condition, $I_M(t) = 0$, due to the external capacitor C_e. In the case of small external and intrinsic device capacitance, the response is instantaneous and the potential level "follows" the magnetization direction [6]. The transient current response depends on the RC of the system and on the spin-accumulation profile in the nonmagnetic layer, which is modeled here by a graphene sheet. The use of graphene provides a robust room temperature spin-accumulation signal [10], i.e., several orders of magnitude greater than in currently available silicon devices [11].

Another novelty in the MLG design of Fig. 1 is the spin-transfer torque (STT) magnetization writing [12], [13]. Each contact employs an all-metallic three-terminal path for the writing current I_w [14]. This path allows significant energy savings compared with tunneling-based STT pillar techniques [15], [16] in which the writing current flows through tunnel barriers. In the writing scheme depicted in Fig. 1, the magnetic moment of the free layer (Py) of a logic operand contact (A–D) is switched by applying a nanosecond-scale current pulse $I_w(t)$ between the two top CoFe layers of the contact. The magnetization directions of all CoFe regions are fixed (hard layers). A write current pulse in the opposite direction switches the magnetic moment of the free layer to the opposite orientation. The favorable power scaling with reducing the contact area in STT schemes [17] is an important benefit of MLGs. The area of an MLG can be of the order of 0.01 μm^2 if each STT contact consumes $\sim 50 \times 50$ nm^2 [18]. This area can be further reduced if one uses contacts made of highly anisotropic magnetic materials [19]–[22]. In a search engine, N $\ggg$ 1 gates share two bit-line currents, which write the search bit (A and D), and $\ell \gg 1$ gates share a match-line current that triggers the readout (M). These writing (reading) operations are made simultaneously to N (ℓ) MLGs so that the current direction in each line is controlled by a single switch.

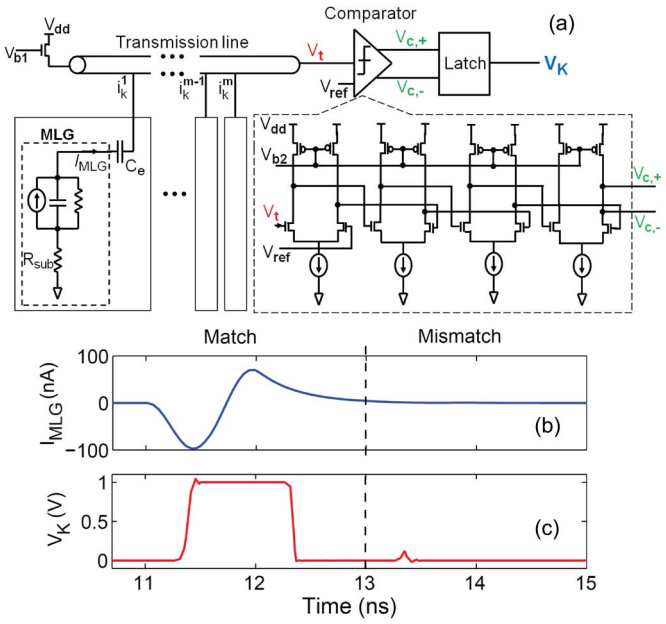

Fig. 3. Circuit schematic for performance evaluation of a spintronic search engine. The MLG model is shown in the dash-line box. The resistance and capacitance in parallel to the current source are 200 kΩ and 0.4 fF, respectively, representing the intrinsic components of the M contact in the MLG. The substrate resistance $R_{\rm sub} = 100$ kΩ denotes the MLG's distributed resistance to the ground (via the graphene layer and the grounded B and C contacts). The coupling capacitor is $C_e = 1$ fF. (b) Current signal at the MLG output prior to the external capacitor. (c) Digital voltage output of the latch V_K from Advanced Design System simulation. The graphs show a match case (between 11 and 13 ns) followed by the worst case mismatch scenario. The former (latter) corresponds to cases where 128 (127) out of 128 bits match.

The readout operation of an MLG is simulated during a 1-ns in-plane full rotation of the magnetization of the middle contact. The bias setting in this single-gate modeling are: A and D are held at $V_{dd} = 1$ V, whereas the match line and B and C are grounded (see Fig. 1). The output current (I_M) is shown in Fig. 2. If the search key (encoded in A & D) matches/mismatches the stored bit (encoded in B and C), then the transient response is significantly larger/smaller. We duplicate the encoding of the search and stored bits in two contacts each in order to account for the possibility of 'do not care' bits. The response in Fig. 2 is modeled via a diffusive transport model in the graphene layer, which includes the effects of traversing under the finite width of the metal contacts [23] and of the intrinsic capacitance across the tunneling barrier [6]. Complete details of the transport model are given in the supplementary material of [2]. We have used the experimental results in [10] and [24] and have assumed the following parameters. The contact spin polarization, areal conductance, and areal capacitance are, respectively, 30%, 10^5 Ω^{-1}cm^{-2}, and 0.08 F/m^2. The sheet resistance in the graphene layer is 1 kΩ, the spin-diffusion length is 3 μm, and the diffusion constant is 0.018 m^2/s (see [6, Fig. 4(a)]).

To demonstrate the potential of MLG-based circuits, we use them as building blocks of a spintronic search engine. The associative search of MLGs enables a highly scalable architecture with low-power consumption. Fig. 3(a) shows a match line circuitry in a spin-based search engine. Each line consists of $\ell = 128$ MLG gates attached to a single transmission line.

The MLG output port is modeled as a pulse current source and a parasitic resistance and capacitance of the M contact. It also includes a distributed resistance $R_{\rm sub}$ from the M contact to the ground (via the graphene layer and contacts B and C). A coupling capacitor C_e is used to isolate the M contact from the CMOS circuitry in dc, and its value is selected as a tradeoff between signal attenuation and the chip area required to implement it on-chip. When the output is short-circuit to ground through C_e, this model reproduces the MLG transient response [compare Figs. 2 and 3(b)].

The output current pulses of all cells are summed on the transmission line. This approach is different from the direct logic wire–OR structure in CMOS search engines, in that each MLG behaves similar to a current source instead of a switch, and exhibits a large impedance to the transmission line in either match or mismatch cases. The high impedance also helps to reduce the crosstalk between the MLGs. The summed current pulses on the transmission line generate a voltage signal at the end of the transmission line (V_t in Fig. 3). This voltage signal goes to an n-stage comparator ($n = 4$ in this design example) in which the other input is $V_{\rm ref}$. This reference voltage simulates the worst case scenario in which 127 out of 128 bits are matched and the current signal of one bit is halfway between a match and a mismatch. At the output of the comparator, a latch converts the signal to a full-swing digital signal, indicating a match or mismatch. The comparator is optimized for a small offset voltage and a large common-mode rejection ratio, which reduce the comparison error. This low-noise analog sensing circuit exhibits good sensitivity and fine resolution with power consumption comparable with a conventional sense amplifier in SRAMs. The prototype circuit is simulated using a high-speed circuit simulator (Advanced Design System). The CMOS transistors are based on 45-nm predictive technology model [25], and the power supply voltage is $V_{dd} = 1$ V. Fig. 3(c) shows the match/mismatch output of the final digital latch.

The simulated 128-bit match-line sensing circuit operates at 500 MHz and detects an MLG output current difference down to 9 nA. The four-stage comparator and the latch use 0.26 mW. For a 3.2-Mbit search engine (25 000 words of 128 bits), the total power consumption of these CMOS circuitry is 6.5 W. The power dissipation of each MLG is mostly due to the dc current that flow between the A and B contacts as well as the C and D contacts. In our simulated 200-KΩ contacts and $V_{\rm dd} = 1$ V applied bias, this corresponds to 5 μW per MLG (16 W for 3.2-Mbit search engine). Together with the (much smaller) power consumption of all latches in the sensing circuits and the STT-writing operations, the total power consumption of the MLG-based search engine is about 23 W. However, improved tunneling barriers in the MLG will keep the MLG current output at the same magnitude but will use less power. For example, the entire circuit power consumption drops to 9 W if smaller MLG contacts with a resistance of $R = 2$ MΩ and spin polarization of 90% can be fabricated. In this case, the performance of the improved MLG (size and power) is considerably enhanced compared with optimized 32-nm CMOS counterpart designs [26].

In conclusion, we presented a search engine circuit whose building blocks are MLG devices. This circuit is scalable, and it offers high-speed operation at low-power dissipation. It is envisioned that graphene can achieve enhanced performance at room temperature. The application of spin-based devices [2], [5] in nonvolatile logic circuits will represent a disruptive advance in the design and implementation of critical building blocks in high-performance computing and communication systems. Fundamentally, it will enable a paradigm change from the von Neumann architecture to one in which memory and processing are seamlessly integrated together.

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