A Read-Out Integrated Circuit for a Satellite-mounted Mid-Wave Image Sensor

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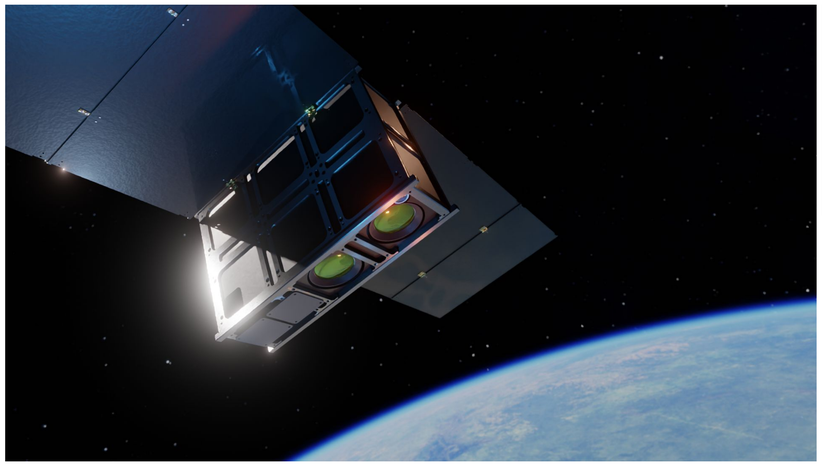
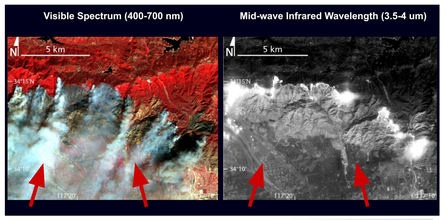
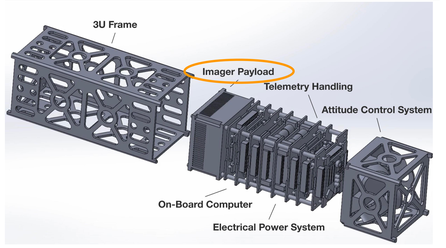
Motivation

Wildfires are some of the most destructive natural disasters in forested regions around the globe. Every year, wildfires burn an average of **7 million acres** of American land, and last year the department of the interior allocated **$1.5 billion** on wildfire response alone. Early prevention is by far the most important factor in the fight against this destruction, so there is a strong need (and a rich market) for a technological solution.







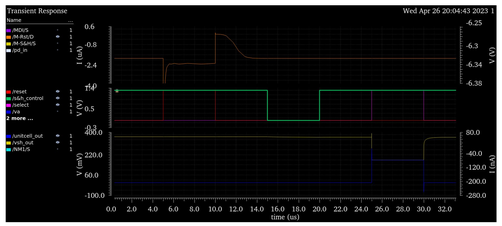
Enter MILDFIRE: a midwave imager and cubesat constellation purpose-built for early wildfire detection. Midwave IR imaging is selected because it allows the camera to pierce through the smoke, but there are very few midwave readout IC's capable of withstanding satellite environments. Our integrated circuit design uses generic 90nm SOI fabrication specifications, to verify this proof-of-concept imaging system.

Industry standard Cadence Virtuoso schematic and layout software was utilized in three discrete stages, which when combined represent the entire readout circuitry attached to the imager's photodiode array. Through this work, we are one step closer to realizing this cost-effective and efficient satellite constellation.

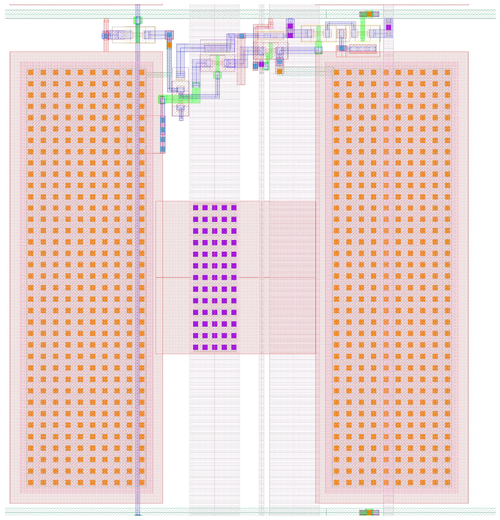
Stage 1: Unit Cell

The unit cell is mounted below each individual pixel's photodiode. It integrates and amplifies the weak signal coming from the photodiode. After the light for one frame has been integrated, the voltage is transferred to a sample-and-hold stage, so it can be read out while the next frame is being captured. The control scheme is flexible and allows correlated double sampling to be used to reduce noise.

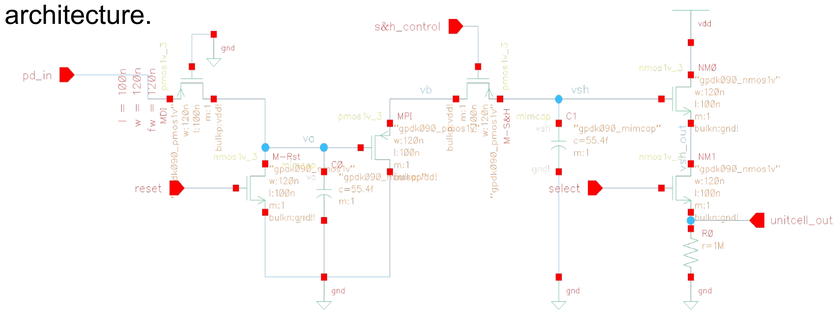
The two rectangles on the sides of the cell are the integration and S&H capacitors, which are some of the most important components in the cell, and need to be as large as possible to keep a steady reading. Though these plates are only about 50fF, simulation verifies that there is a less than 1% loss in signal quality as a result of this architecture.



Simulated output of the unit cell.



Layout of the unit cell.

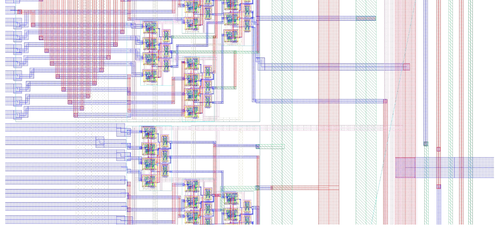


Schematic of the unit cell.

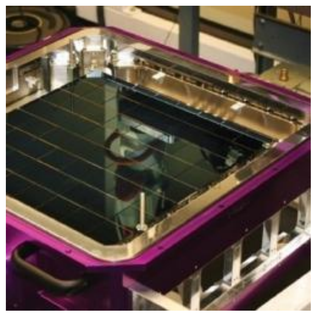
Stage 2: Analog Multiplexer

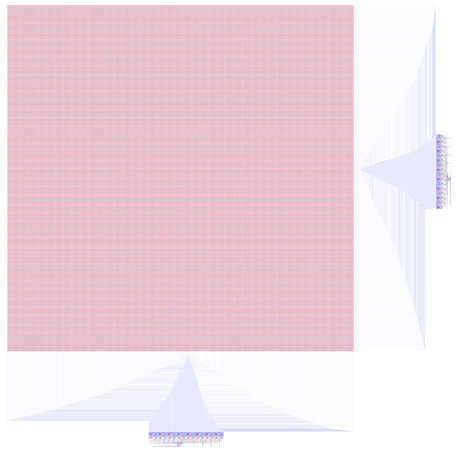
To read out the signals, each column is selected one by one by a demultiplexer. Then each pixel in the column is selected by an analog multiplexer onto a single shared bus so the pixels can be read out one by one.

In order to reduce noise and power consumption caused by switching, both the rows and columns are indexed using Gray code rather than natural binary.



Closeup of the layout of the multiplexer.



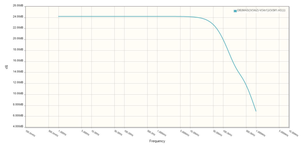


Layout of the entire 256x256 array, with column selector (bottom) and analog multiplexer (right).

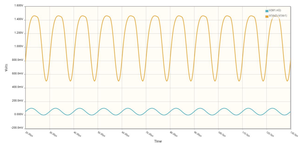
Stage 3: Amplification

This stage primarily serves to amplify the analog signal from each unit cell, providing a high input impedance and low output impedance, in order to preserve the signal while driving an external analog-to-digital converter.

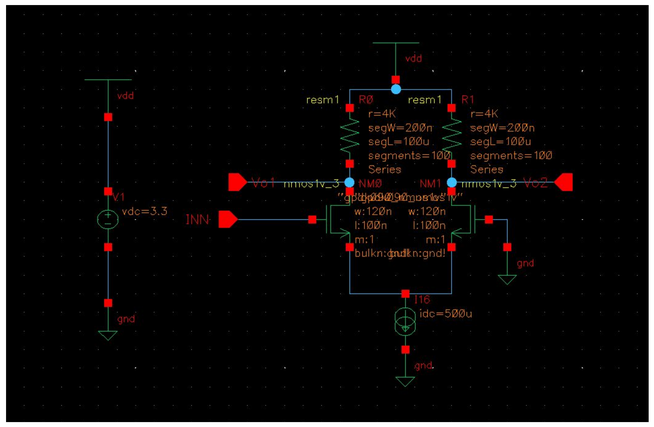
This stage consists of two NMOS transistors that operate as a single-ended to differential converter. The differential output signal helps reduce noise. It operates at a bandwidth of up to 65 kHz with stable 24 dB amplification.



Frequency response of the output amplifier.



Transient output of the output amplifier.



Schematic of the output amplifier.